Features

- ESD protect for two high-speed I/O channels
- Provide transient protection for each channel to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-5 (Lightning) 2.5A (8/20μs)
- **Ultra-low capacitance: 0.18pF typical**
- **For operating voltage of 1.5V and below**
- Fast turn-on and ultra-low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS diode
- Solid-state silicon-avalanche and active circuit triggering technology
- Simplified layout for high-speed differential signaling channels
- ***Green part***

Applications

- **Thunderbolt interface**
- **USB3.1 and USB3.0 interfaces**
- **USB Type-C interface**
- DisplayPort interface
- SATA and eSATA interface
- V-By-One interface
- Consumer electronics

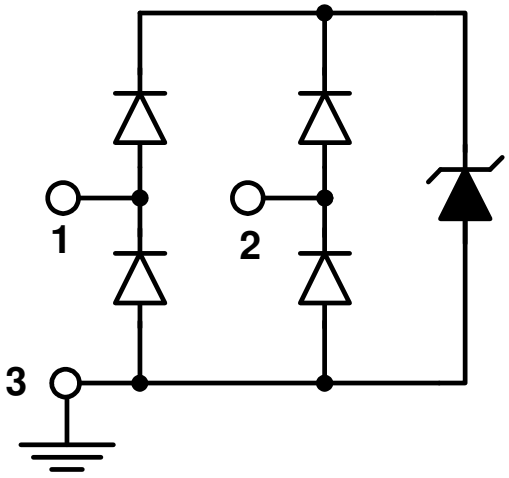
Description

AZ101S-02F is a design which includes ESD rated diode arrays to protect high-speed data interfaces. The AZ101S-02F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD).

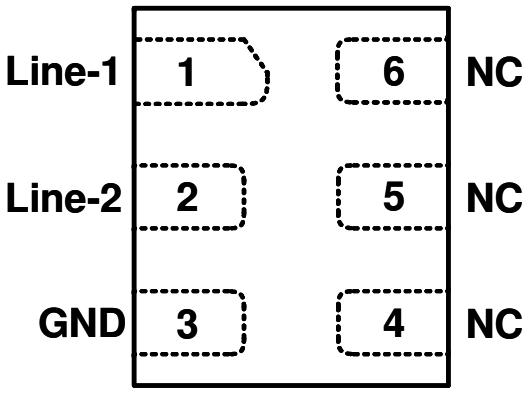
AZ101S-02F is a unique design which includes ESD rated, ultra-low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the internal ESD line or to ground line. The internal unique design of clamping cell prevents over-voltage on the internal ESD line and on the I/O line, which is protecting any downstream components.

AZ101S-02F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



DFN1210P6X (Top View)

SPECIFICATIONS

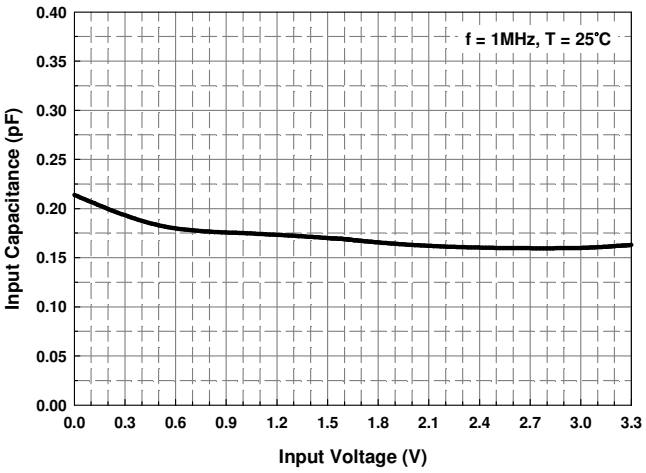
ABSOLUTE MAXIMUM RATINGS (T_A= 25°C, unless otherwise specified)			
PARAMETER	**SYMBOL**	**RATING**	**UNIT**
Peak Pulse Current (tp =8/20μs)	I_{PP}	2.5	A
Operating Voltage (I/O pin-GND)	V_{DC}	1.65	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±15 ±8	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1,-2 to pin-3, T=25 °C.			1.5	V
Channel Leakage Current	$I_{CH-Leak}$	$V_{Pin-1,-2}$ = 1.5V, V_{Pin-3} = 0V, T=25 °C.			0.5	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, pin-1, -2 to pin-3.	4.5			V
Forward Voltage	V_F	I_F = 15mA, T=25 °C, pin-3 to pin-1, -2.		0.9	1.1	V
ESD Clamping Voltage (Note 1)	V_{CL-ESD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), Contact mode, T=25 °C, any I/O pin to GND.		12		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0 ~ +8kV, Contact mode, T=25 °C, any I/O pin to GND.		0.55		Ω
Channel Input Capacitance	C_{IN}	V_{Pin-3} = 0V, V_{IN} = 1.0V, f = 1MHz, T=25 °C, any I/O pin to GND.		0.18	0.28	pF
Channel to Channel Input Capacitance	C_{CROSS}	V_{Pin-3} = 0V, V_{IN} = 1.0V, f = 1MHz, T=25 °C, between I/O pins.		0.05	0.08	pF

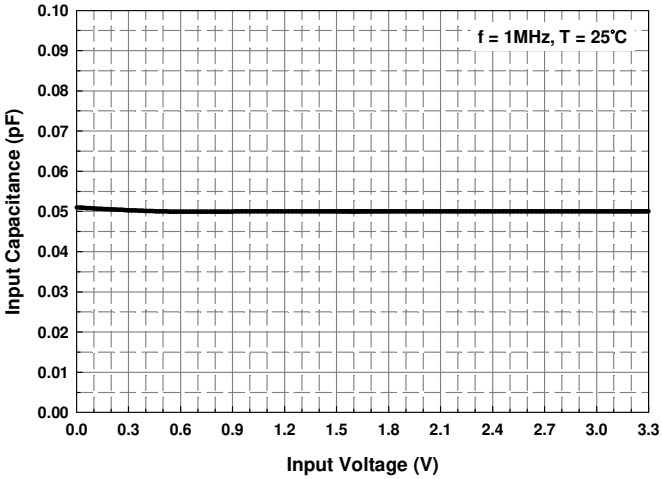
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

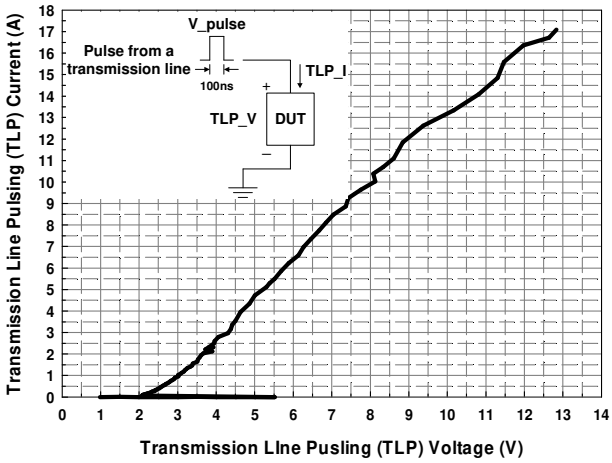
Typical Variation of C_{IN} vs. V_{IN}



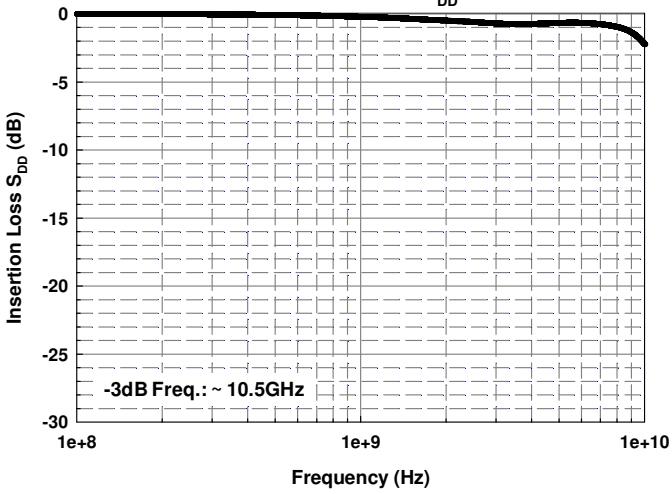
Typical Variation of $C_{IO\text{-}to\text{-}IO}$ vs. V_{IN}



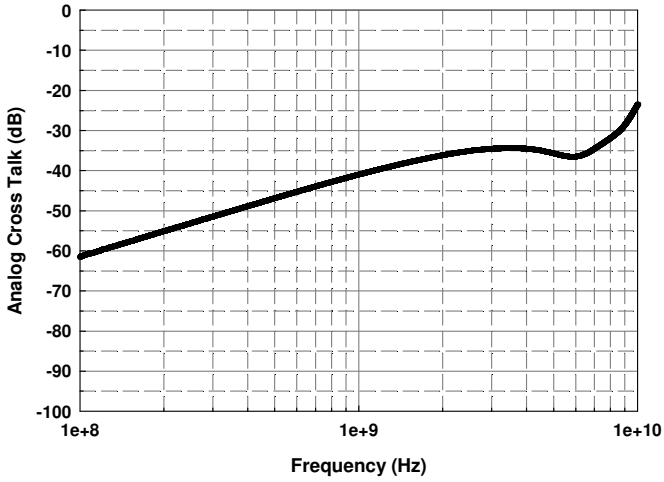
Transmission Line Pulsing (TLP) Measurement



Insertion Loss S_{DD}



Analog Cross Talk



Application Information

A. Device Connection

The AZ101S-02F is designed to protect two data lines from transient over-voltage (such as ESD stress pulse). The device connection of AZ101S-02F is shown in the Fig. 1. In Fig. 1, the two protected data lines are connected to the ESD protection pins (pin1, pin2) of AZ101S-02F. The ground pin (pin3) of AZ101S-02F is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible.

AZ101S-02F can provide protection for 2 I/O signal lines simultaneously. If the number of I/O signal lines is less than 2, the unused I/O pins can be simply left as NC pins.

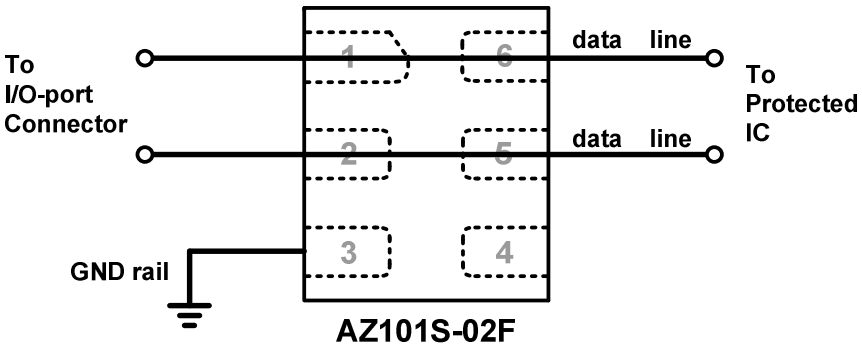
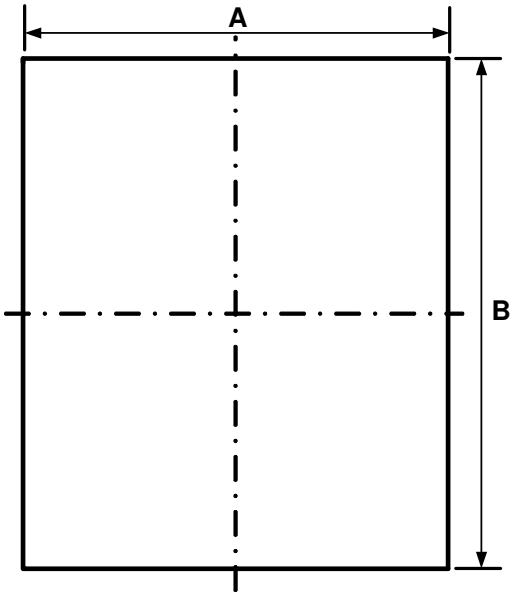


Fig. 1 Data lines connection of AZ101S-02F.

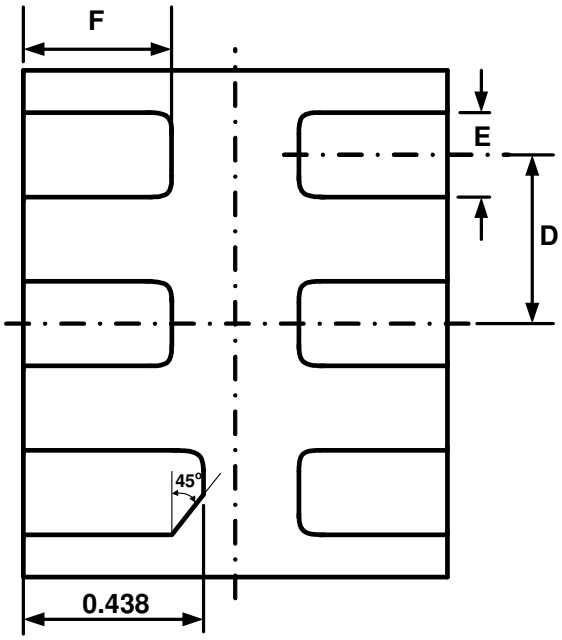
Mechanical Details

DFN1210P6X

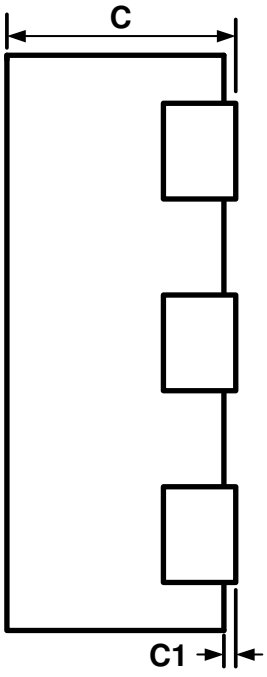
PACKAGE DIAGRAMS AND DIMENSIONS



TOP VIEW



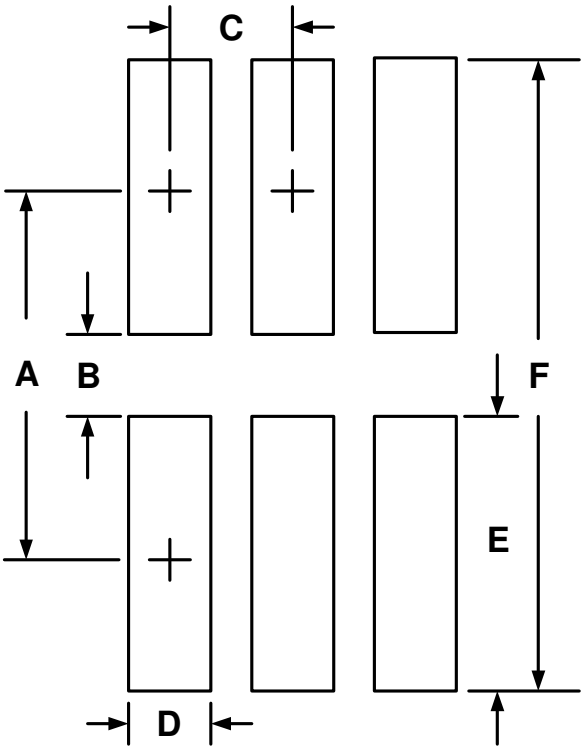
BOTTOM VIEW (unit in mm)



SIDE VIEW

SYMBOL	Millimeters		
	MIN.	NOM.	MAX.
A	0.95	1.00	1.05
B	1.15	1.20	1.25
C	0.41	0.45	0.50
C1	0.00	0.02	0.05
D		0.40	
E	0.15	0.20	0.25
F	0.25	0.35	0.45

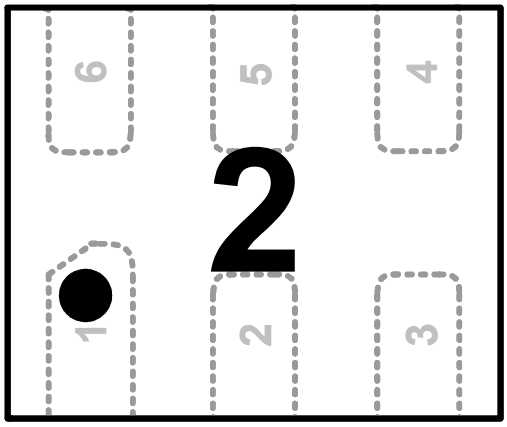
LAND LAYOUT



Dimensions		
Index	Millimeter	Inches
A	0.875	0.034
B	0.20	0.008
C	0.40	0.016
D	0.20	0.008
E	0.675	0.027
F	1.55	0.061

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



2 = Device Code

Part Number	Marking Code
AZ101S-02F.R7G (Green Part)	2

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ101S-02F.R7G	Green	T/R	7 inch	3,000/reel	4 reels = 12,000/box	6 boxes =72,000/carton

Revision History

Revision	Modification Description
Revision 2016/02/03	Preliminary Release.
Revision 2018/03/14	Formal Release.