

HIGH POWER DPDT SWITCH GaAs MMIC

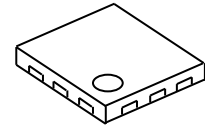
■ GENERAL DESCRIPTION

The NJG1812ME4 is a GaAs DPDT switch MMIC suitable for antenna swapping of LTE/UMTS/CDMA/GSM applications.

The NJG1812ME4 features very low insertion loss, low distortion and excellent linearity performance down to 1.8V 1bit control voltage at high frequency up to 3GHz. In addition, this switch is able to handle high power signals.

The NJG1812ME4 has ESD protection devices to achieve excellent ESD performances. No DC Blocking capacitors are required for all RF ports unless DC is biased externally. And the small & thin EQFN12-E4 package is adopted.

■ PACKAGE OUTLINE



NJG1812ME4

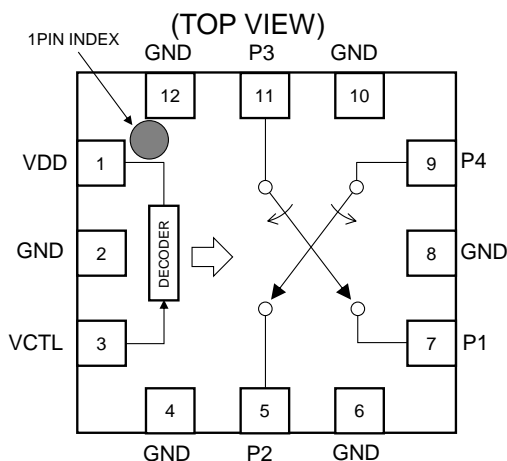
■ APPLICATIONS

Antenna swapping, General purpose switching applications
 LTE, UMTS, CDMA, GSM systems

■ FEATURES

- Low voltage logic control
 - Low voltage operation
 - Low insertion loss
 - Low distortion
 - $P_{-0.1dB}$
 - Ultra-small and ultra-thin package
 - RoHS compliant and Halogen Free, MSL1
- $V_{CTL(H)}=1.35V$ to $5.0V$
 $V_{DD}=2.7V$ typ.
 $0.25dB$ typ. @ $f=900MHz$, $P_{IN}=+35dBm$
 $0.35dB$ typ. @ $f=1900MHz$, $P_{IN}=+33dBm$
 $0.45dB$ typ. @ $f=2700MHz$, $P_{IN}=+27dBm$
 $2nd$ harmonics= $-89dBm$ typ. @ $f=786.5MHz$, $P_{IN}=+23dBm$
 $3rd$ harmonics= $-89dBm$ typ. @ $f=710MHz$, $P_{IN}=+23dBm$
 $+36$ dBm min.
 EQFN12-E4 (Package size: $2.0 \times 2.0 \times 0.397$ mm typ.)

■ PIN CONFIGURATION



Pin connection

- | | |
|---------|-------------|
| 1. VDD | 7. P1 |
| 2. GND | 8. NC(GND) |
| 3. VCTL | 9. P4 |
| 4. GND | 10. NC(GND) |
| 5. P2 | 11. P3 |
| 6. GND | 12. GND |
- Exposed PAD: GND

■ TRUTH TABLE

“H”= $V_{CTL(H)}$, “L”= $V_{CTL(L)}$

VCTL	Path
L	P1-P4 P2-P3
H	P1-P3 P2-P4

■ ABSOLUTE MAXIMUM RATINGS

$T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	P_{IN}	$V_{DD}=2.7\text{V}$, $V_{CTL}=0/1.8\text{V}$	+38	dBm
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	VCTL terminal	5.0	V
Power Dissipation	P_D	Four-layer FR4 PCB with through-hole (101.5 x 114.5mm), $T_j=150^{\circ}\text{C}$	1200	mW
Operating Temp.	T_{opr}		-40 to +105	$^{\circ}\text{C}$
Storage Temp.	T_{stg}		-55 to +150	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS 1 (DC)

(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(H)}=1.8\text{V}$, $V_{CTL(L)}=0\text{V}$, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	VDD Terminal	2.4	2.7	5.0	V
Operating Current	I_{DD}	No RF input	-	90	180	μA
Control Voltage (LOW)	$V_{CTL(L)}$	VCTL Terminal	0	-	0.45	V
Control Voltage (HIGH)	$V_{CTL(H)}$	VCTL Terminal	1.35	1.8	5.0	V
Control Current	I_{CTL}	$V_{CTL(H)}=1.8\text{V}$	-	4	10	μA

■ ELECTRICAL CHARACTERISTICS 2 (RF)

(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(H)}=1.8\text{V}$, $V_{CTL(L)}=0\text{V}$, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss 1	LOSS1	f=900MHz, $P_{IN}=+35\text{dBm}$	-	0.25	0.45	dB
Insertion Loss 2	LOSS2	f=1900MHz, $P_{IN}=+33\text{dBm}$	-	0.35	0.55	dB
Insertion Loss 3	LOSS3	f=2700MHz, $P_{IN}=+27\text{dBm}$	-	0.45	0.65	dB
Isolation 1	ISL1	f=900MHz, $P_{IN}=+35\text{dBm}$	23	25	-	dB
Isolation 2	ISL2	f=1900MHz, $P_{IN}=+33\text{dBm}$	18	20	-	dB
Isolation 3	ISL3	f=2700MHz, $P_{IN}=+27\text{dBm}$	15	17	-	dB
Input Power at 0.1dB Compression Point	$P_{-0.1\text{dB}}$	f=900MHz, 1900MHz, 2700MHz	+36	-	-	dBm
VSWR	VSWR	P1 to P4 Terminal, f=2700MHz	-	1.1	1.5	-
Switching time	T_{SW}	50% V_{CTL} to 10/90% RF	-	1	5	μs

■ ELECTRICAL CHARACTERISTICS 2 (RF)

(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(H)}=1.8\text{V}$, $V_{CTL(L)}=0\text{V}$, with application circuit)

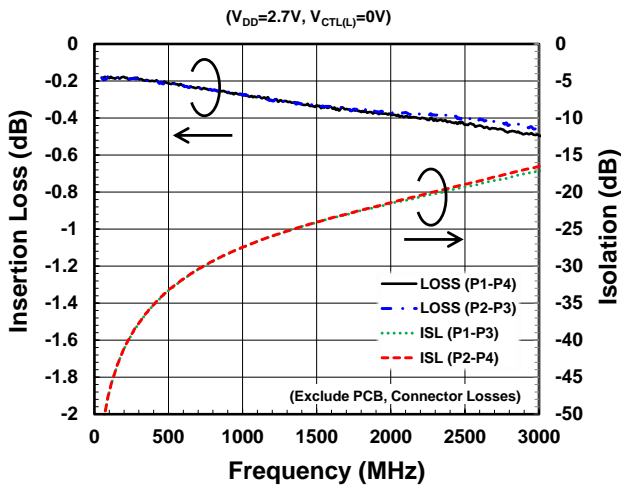
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
2nd Harmonics 1	2fo(1)	f=900MHz, P _{IN} =+33dBm	-	-	-40	dBm
2nd Harmonics 2	2fo(2)	f=1900MHz, P _{IN} =+30dBm	-	-	-40	dBm
2nd Harmonics 3	2fo(3)	f=2700MHz, P _{IN} =+23dBm	-	-	-60	dBm
2nd Harmonics 4	2fo(4)	f=786.5MHz, P _{IN} =+23dBm		-89	-81	dBm
3rd Harmonics 1	3fo(1)	f=900MHz, P _{IN} =+33dBm	-	-	-40	dBm
3rd Harmonics 2	3fo(2)	f=1900MHz, P _{IN} =+30dBm	-	-	-40	dBm
3rd Harmonics 3	3fo(3)	f=2700MHz, P _{IN} =+23dBm	-	-	-60	dBm
3rd Harmonics 4	3fo(4)	f=710MHz, P _{IN} =+23dBm	-	-89	-81	dBm
2nd order intermodulation	IMD2	f _{TX} =835MHz, P _{TX} =+20dBm, f _{jam} =1715MHz, P _{jam} =-15dBm, f _{meas} =880MHz	-	-110	-105	dBm
3rd order intermodulation	IMD3	f _{TX} =835MHz, P _{TX} =+20dBm, f _{jam} =790MHz, P _{jam} =-15dBm, f _{meas} =880MHz	-	-110	-105	dBm
Triple Beat Ratio	TBR	f _{TX1} =835.5MHz, P _{TX1} =+21.5dBm, f _{TX2} =836.5MHz, P _{TX2} =+21.5dBm, f _{jam} =881.5MHz, P _{jam} =-30dBm, f _{meas} =881.5±1MHz	81	-	-	dBc

■ TERMINAL INFORMATION

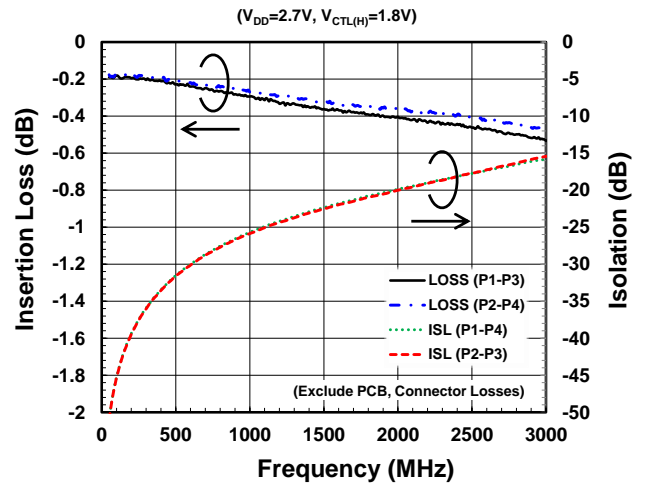
No.	SYMBOL	DESCRIPTION
1	VDD	Positive voltage supply terminal. The positive voltage (+2.4 to +5V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
2	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
3	VCTL	Control signal input terminal. This terminal is set to High-Level (+1.35 to +5.0V) or Low-Level (0 to +0.45V).
4	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
5	P2	RF transmitting/receiving port. No DC blocking capacitor is required for this port unless DC is biased externally. Please connect an inductor with GND terminal for ESD protection.
6	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
7	P1	RF transmitting/receiving port. No DC blocking capacitor is required for this port unless DC is biased externally. Please connect an inductor with GND terminal for ESD protection.
8	NC(GND)	No connected terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
9	P4	RF transmitting/receiving port. No DC blocking capacitor is required for this port unless DC is biased externally.
10	NC(GND)	No connected terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
11	P3	RF transmitting/receiving port. No DC blocking capacitor is required for this port unless DC is biased externally.
12	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
Exposed Pad	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.

■ ELECTRICAL CHARACTERISTICS (With application circuit, loss of external circuit are excluded.)

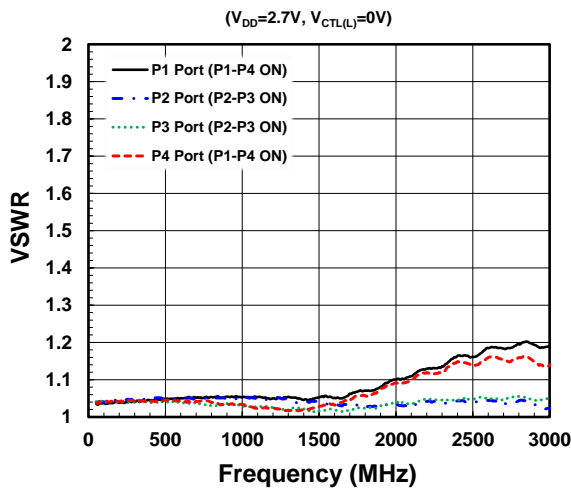
LOSS, ISL vs. Frequency



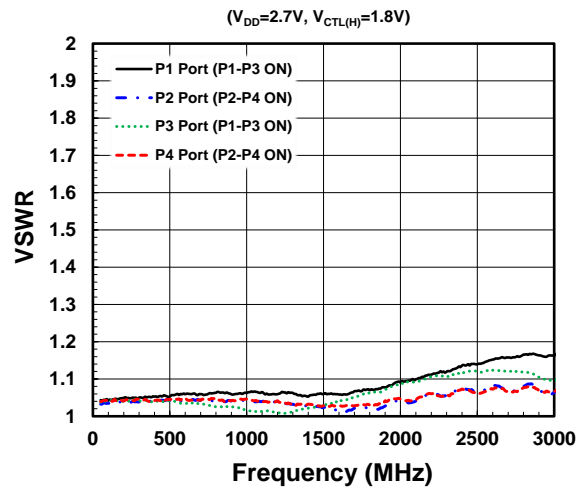
LOSS, ISL vs. Frequency



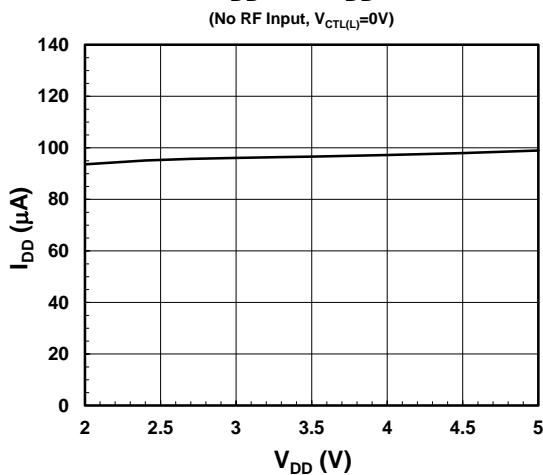
VSWR vs. Frequency



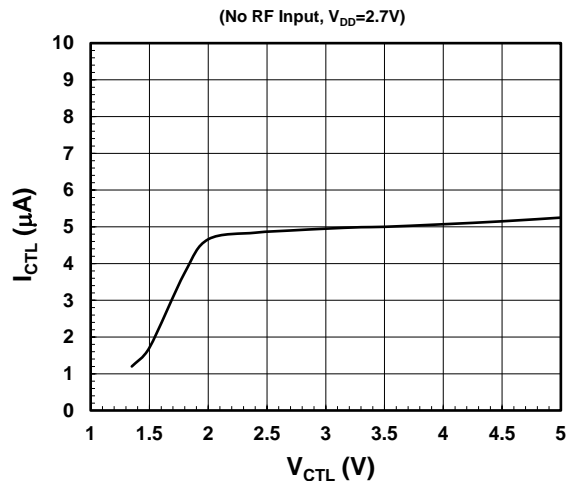
VSWR vs. Frequency



I_{DD} vs. V_{DD}



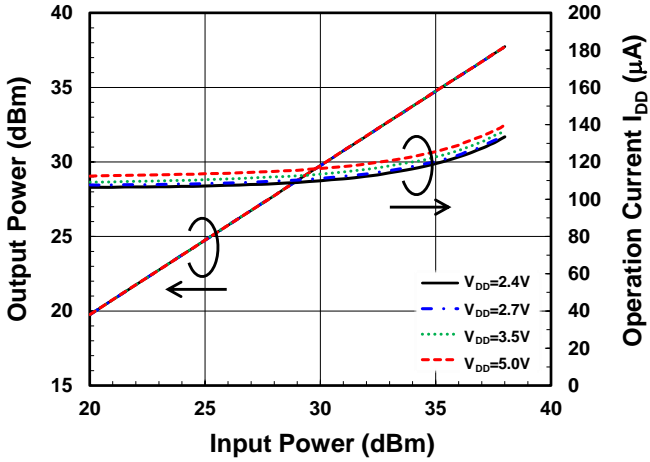
I_{CTL} vs. V_{CTL}



■ ELECTRICAL CHARACTERISTICS (With application circuit, loss of external circuit are excluded.)

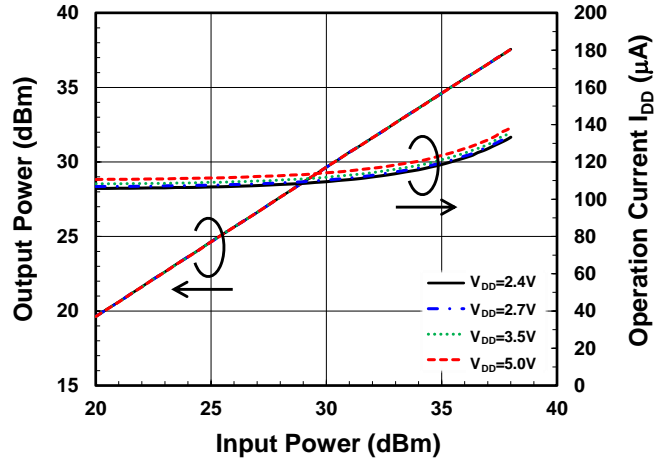
Output Power, I_{DD} vs. Input Power

(f=900MHz, P2-P3 ON, $V_{CTL(L)}=0V$)



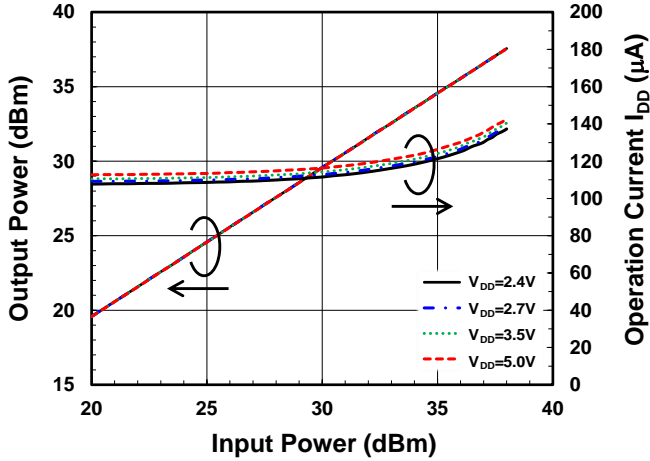
Output Power, I_{DD} vs. Input Power

(f=1900MHz, P2-P3 ON, $V_{CTL(L)}=0V$)



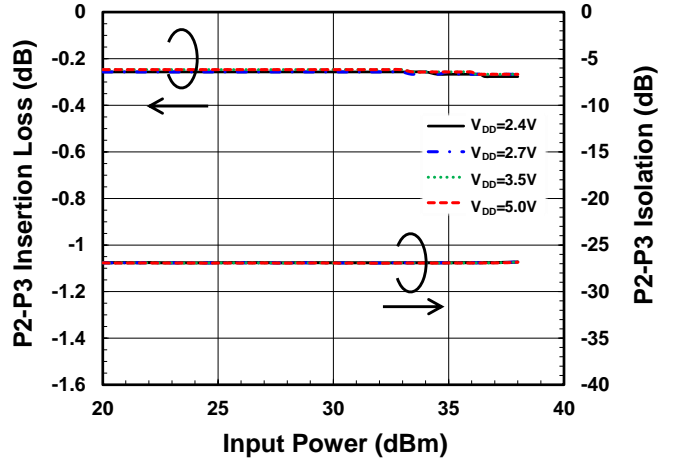
Output Power, I_{DD} vs. Input Power

(f=2700MHz, P2-P3 ON, $V_{CTL(L)}=0V$)



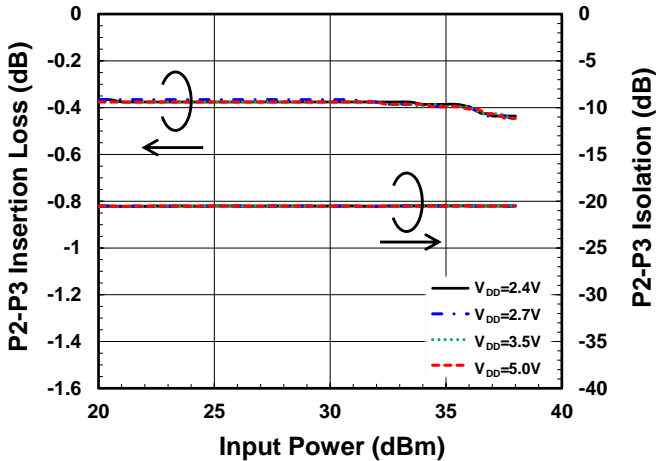
LOSS, ISL vs. Input Power

(f=900MHz, $V_{CTL(L)}=0V$, $V_{CTL(H)}=1.8V$)



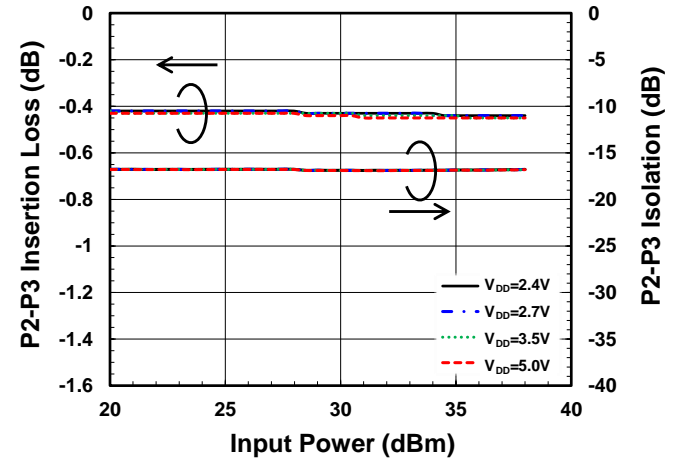
LOSS, ISL vs. Input Power

(f=1900MHz, $V_{CTL(L)}=0V$, $V_{CTL(H)}=1.8V$)

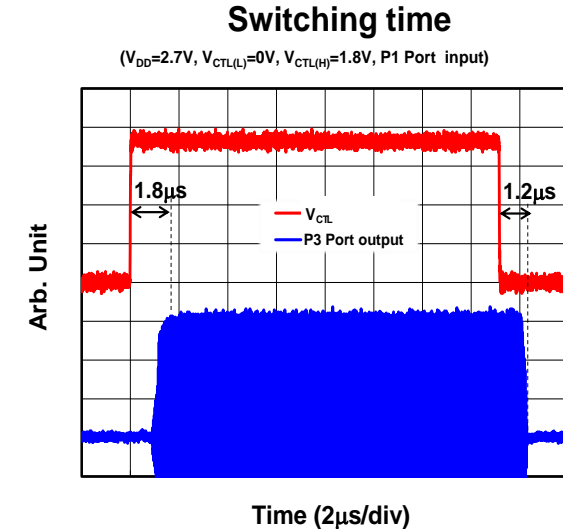
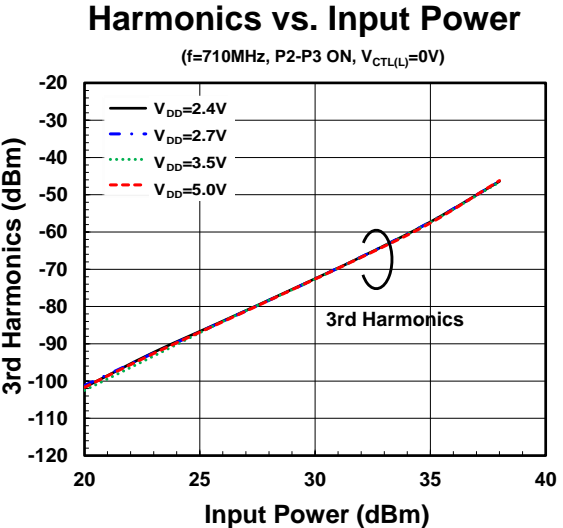
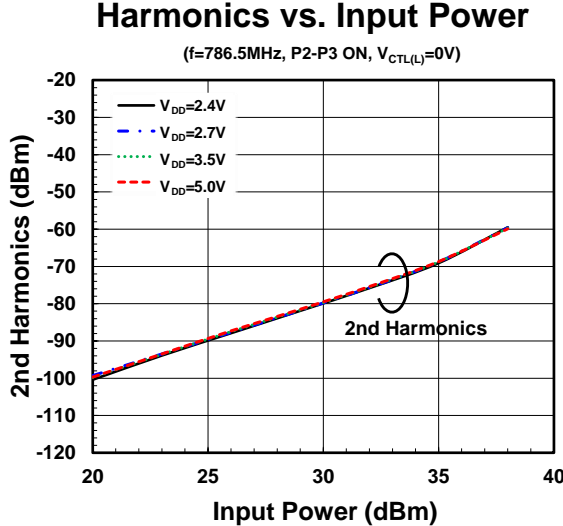
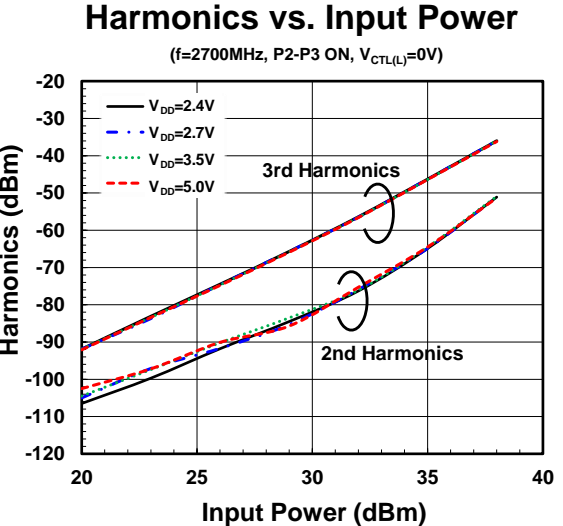
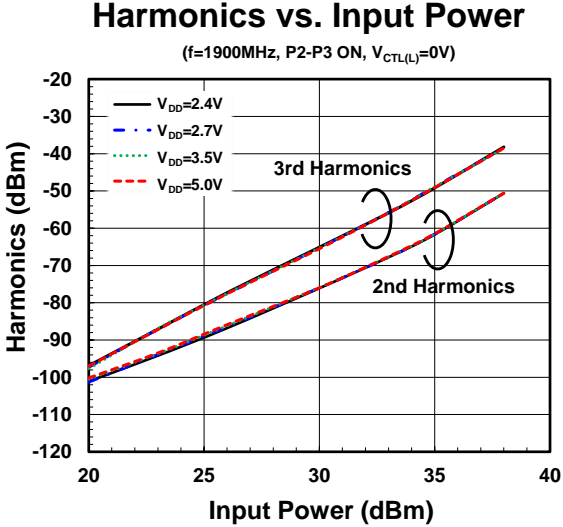
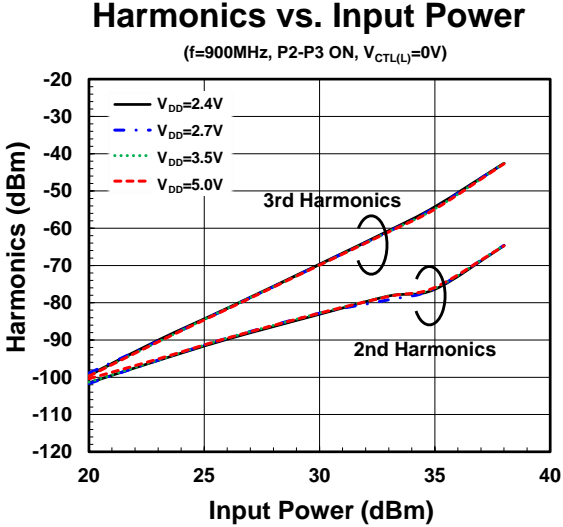


LOSS, ISL vs. Input Power

(f=2700MHz, $V_{CTL(L)}=0V$, $V_{CTL(H)}=1.8V$)

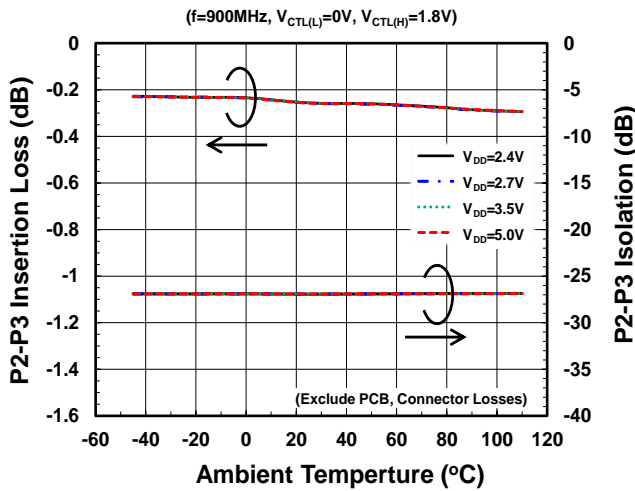


■ ELECTRICAL CHARACTERISTICS (With application circuit, loss of external circuit are excluded.)

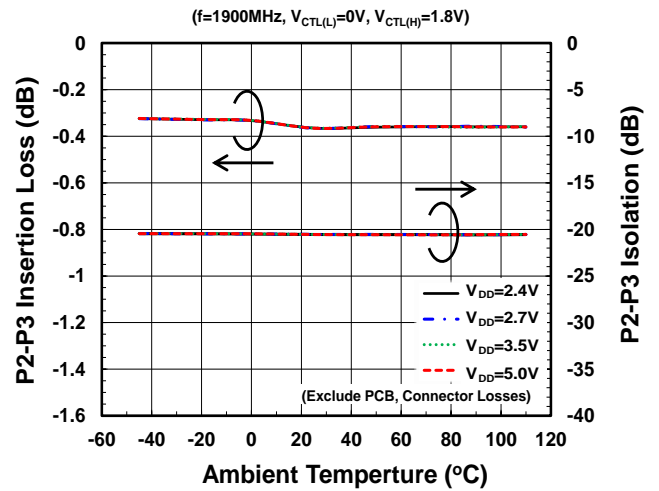


■ ELECTRICAL CHARACTERISTICS (With application circuit, loss of external circuit are excluded.)

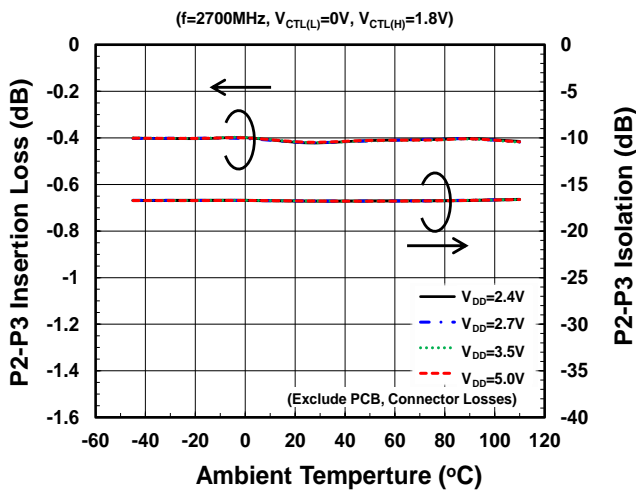
LOSS, ISL vs. Ambient Temperature



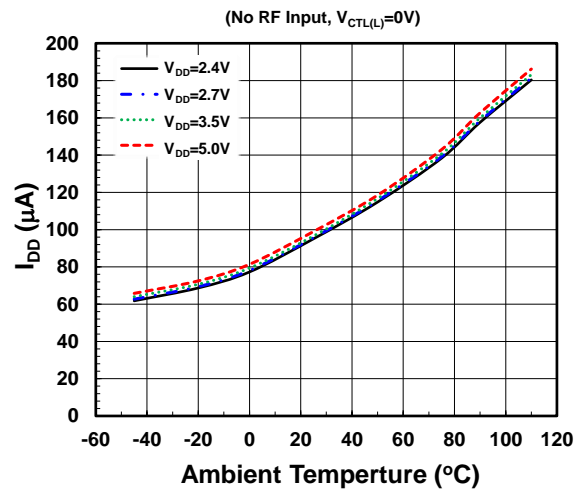
LOSS, ISL vs. Ambient Temperature



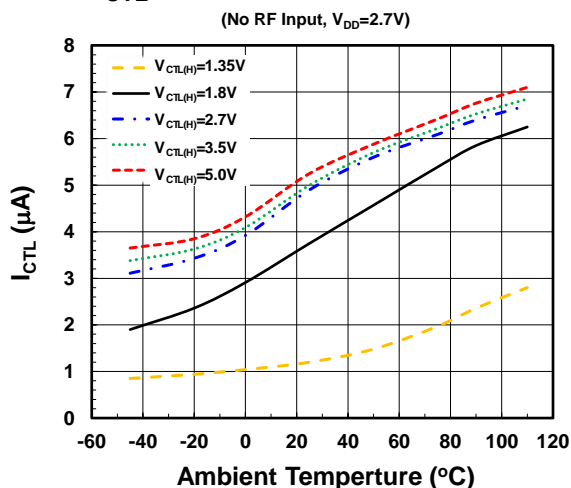
LOSS, ISL vs. Ambient Temperature



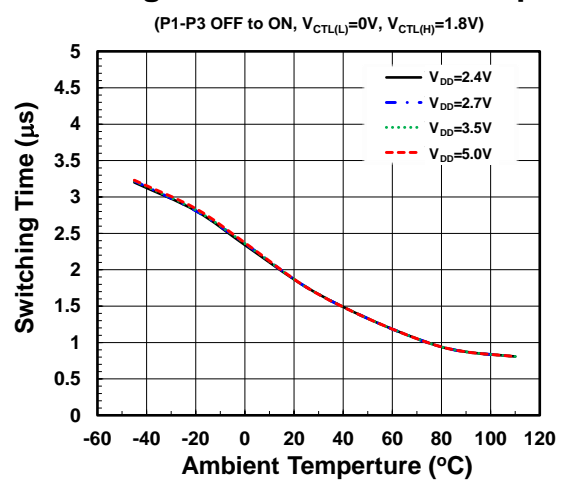
I_{DD} vs. Ambient Temperature



I_{CTL} vs. Ambient Temperature

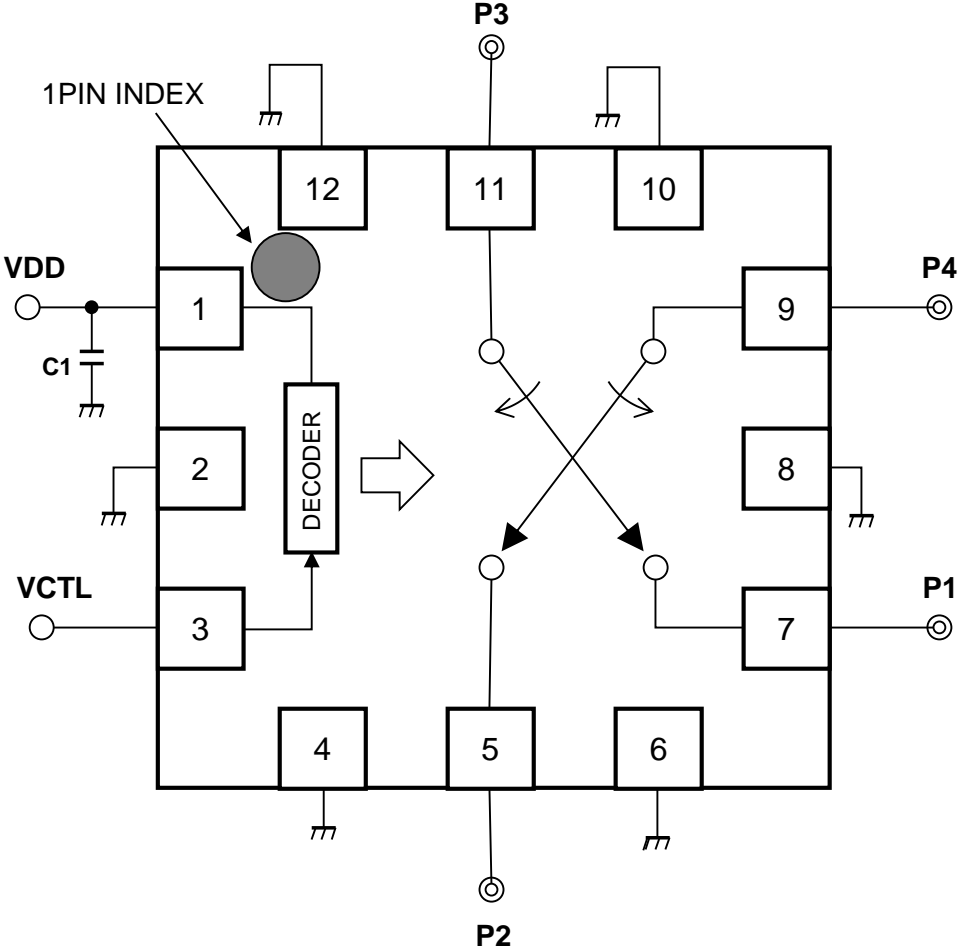


Switching Time vs. Ambient Temperature



■ APPLICATION CIRCUIT

(TOP VIEW)

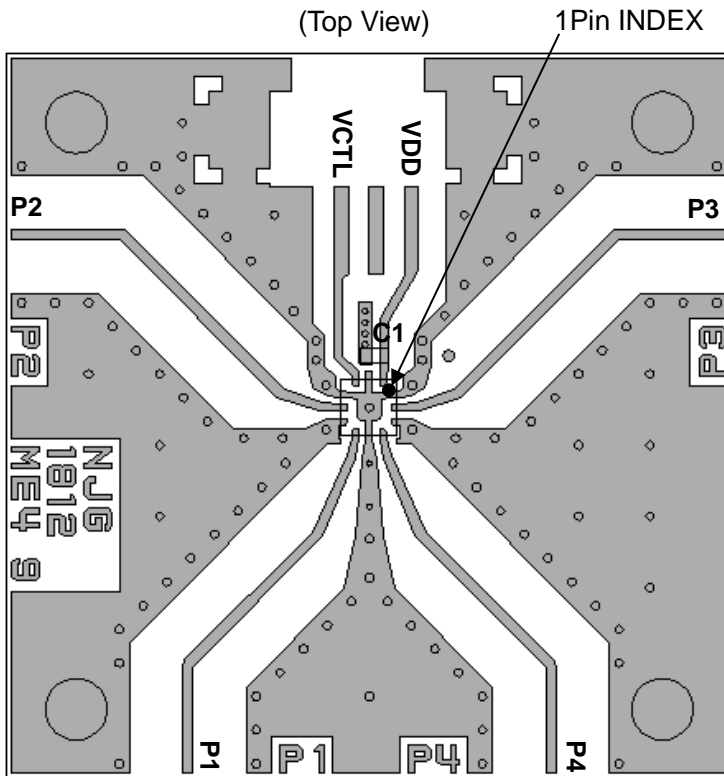


Note: No DC blocking capacitors are required on all RF ports, unless DC is biased externally.

■ PARTS LIST

No.	Parameters	Note
C1	1000pF	MURATA (GRM15)

■ EVALUATION BOARD



PCB (FR-4):

$t=0.2\text{mm}$

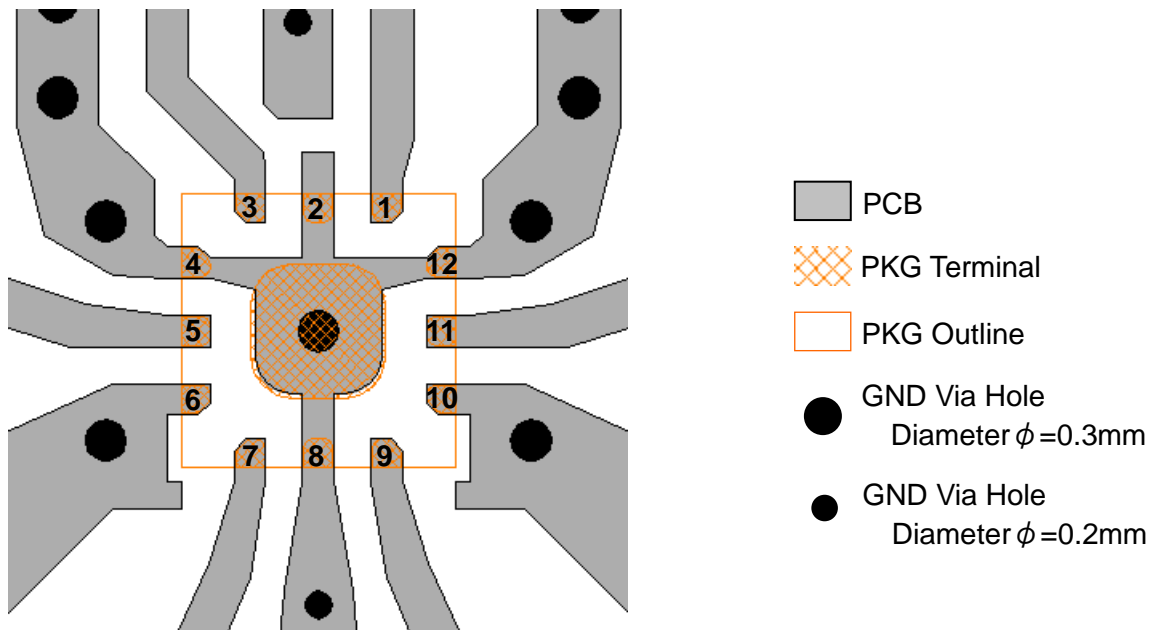
MICROSTRIP LINE WIDTH=0.37mm ($Z_0=50\Omega$)

PCB SIZE=26mm x 26mm

Losses of PCB and connectors, $T_a=+25^\circ\text{C}$

Frequency [GHz]	Loss [dB]
0.9	0.23
1.9	0.43
2.7	0.55

■ PCB LAYOUT GUIDELINE (EQFN12-E4)



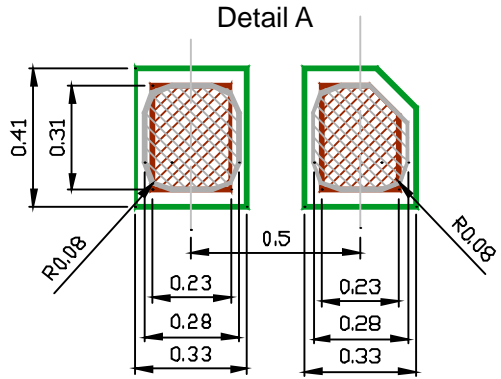
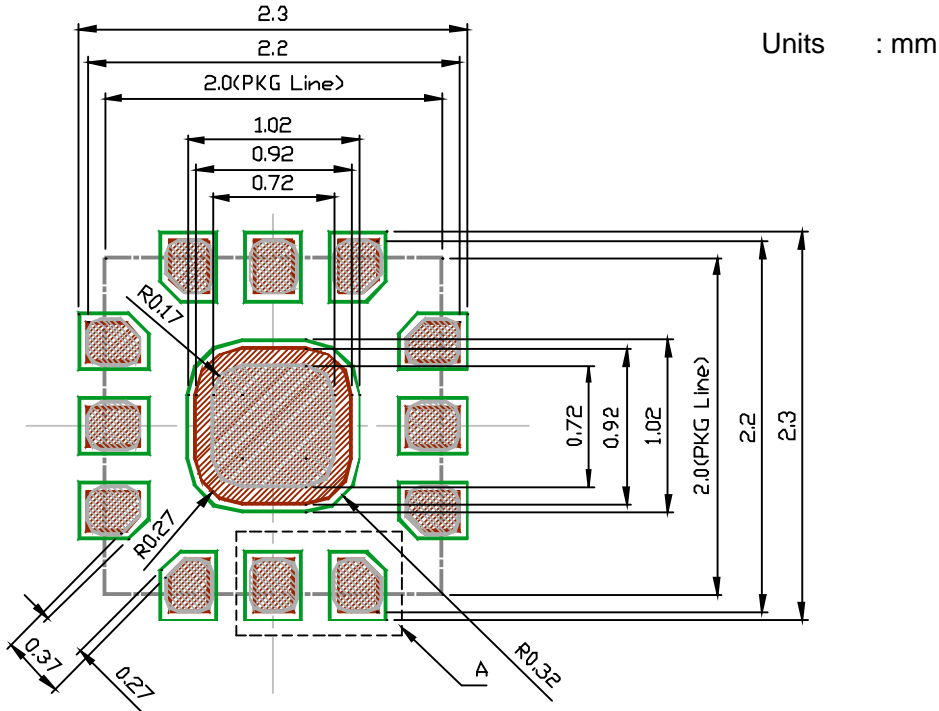
PRECAUTIONS

- [1] For avoiding the degradation of RF performance, the bypass capacitor (C1) should be placed as close as possible to VDD terminal
- [2] For good RF performance, all GND terminals are must be connected to PCB ground plane of substrate, and through - holes for GND should be placed near the IC.
- [3] Please connect Exposed PAD to PCB ground plane of substrate, and through - holes for GND should be placed under the IC.

■ RECOMMENDED FOOTPRINT PATTERN (EQFN12-E4 PACKAGE Reference)

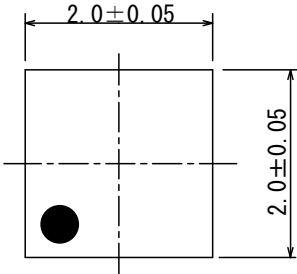
PKG: 2.0mm x 2.0mm
 Pin pitch: 0.5mm

- : Land
- : Mask (Open area) *Metal mask thickness: 100μm
- : Resist (Open area)



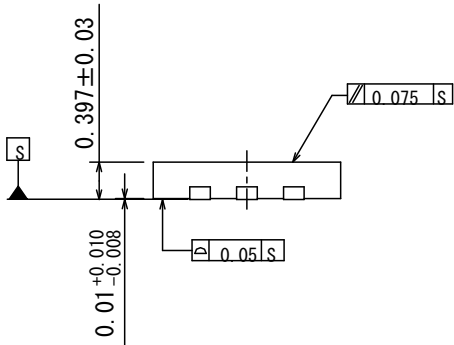
■ PACKAGE OUTLINE (EQFN12-E4)

TOP VIEW

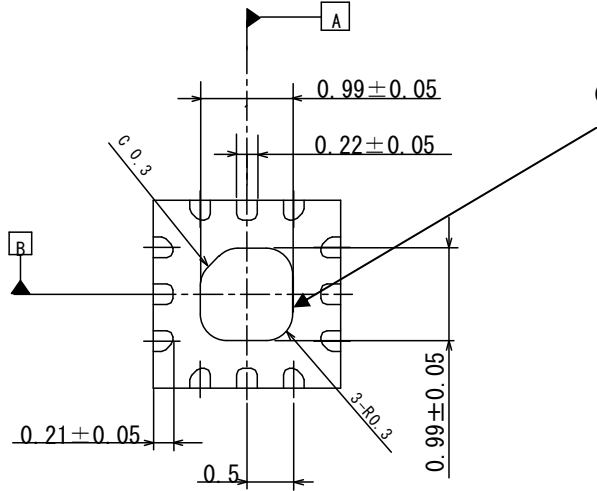


Units	: mm
Board	: Cu
Terminal treat	: SnBi
Molding material	: Epoxy resin
Weight	: 4.7mg

SIDE VIEW



BOTTOM VIEW



Ground connection is required.

Cautions on using this product
 This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

[CAUTION]
 The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.