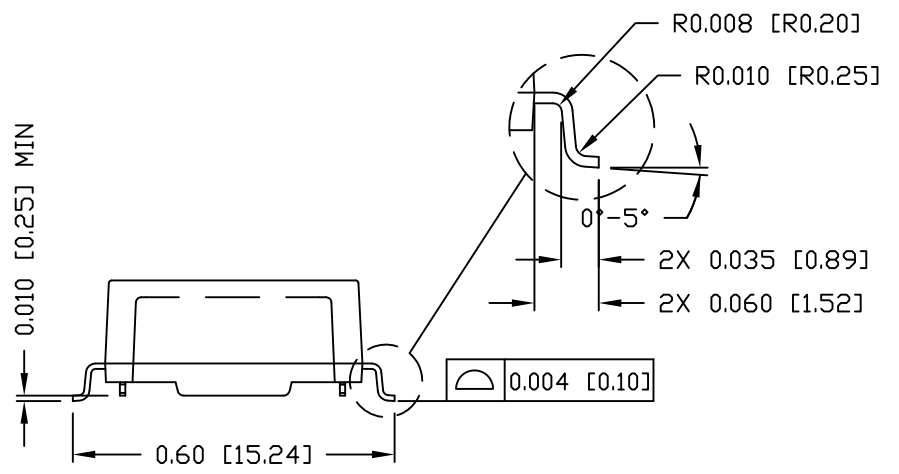
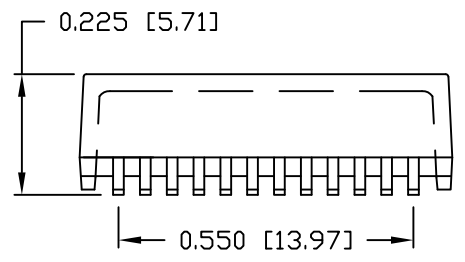
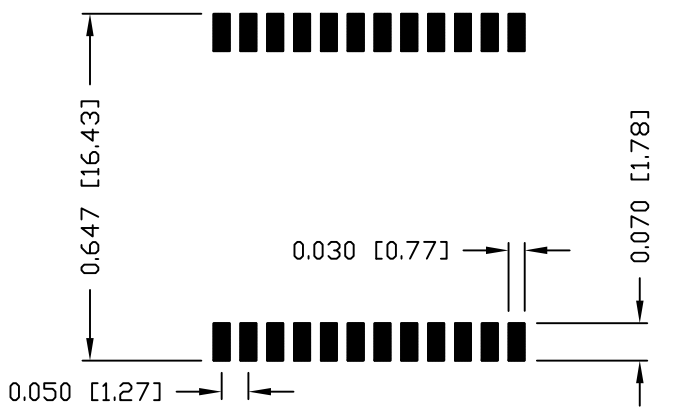
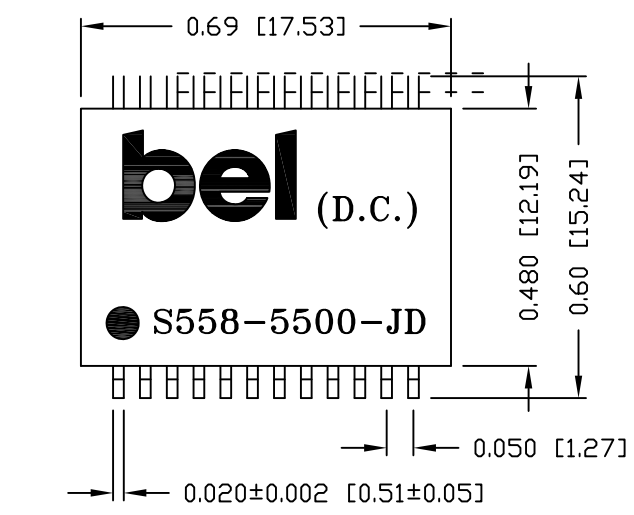


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PRELIMINARY

SUGGESTED PCB PAD LAYOUT



NOTES:

- STANDARD MARKING REFER TO DOC. HAND-WORK-04.
- PACKAGE CODE: "RQS001".

ORIGINATED BY Lawrence Tsang	DATE 2015-12-17	TITLE MECHANICAL OUTLINE	PART NO. / DRAWING NO. S558-5500-JD	STANDARD DIM. TOL. IN INCH	[] METRIC DIM. AS REF.	REV. : PA	PAGE : 3
DRAWN BY ZC Guo	DATE 2015-12-17		FILE NAME S5585500JDPA.DWG	.X /	UNIT : INCH [mm]	 POWER PROTECT CONNECT	
				.XX ±0.01	SCALE : N/A		
			.XXX ±0.005	SIZE : A4			

DC002(2)120214

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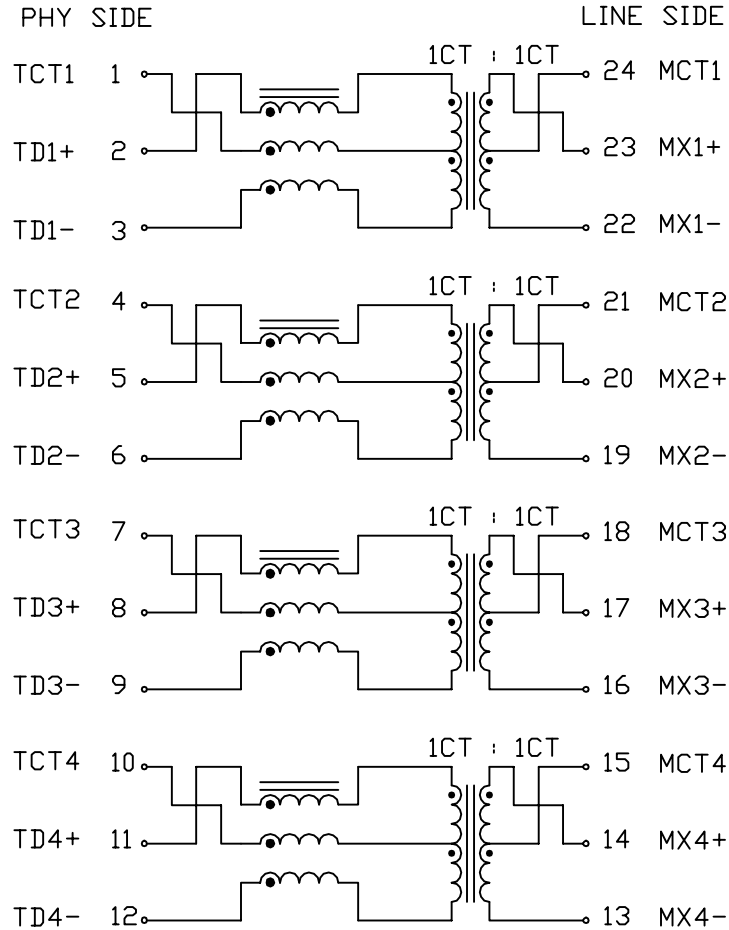
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RoHS



ELECTRICAL CHARACTERISTICS @25°C

SCHEMATIC



URNS RATIO
 (2-1-3) : (23-24-22)
 (5-4-6) : (20-21-19)
 (8-7-9) : (17-18-16)
 (11-10-12) : (14-15-13)

1CT : 1CT ±2%
 1CT : 1CT ±2%
 1CT : 1CT ±2%
 1CT : 1CT ±2%

POLARITY

PER DOT CONVENTION

DCL
 0°C TO 70°C
 0°C TO 70°C

100kHz, 100mV
 180µH MIN WITH 8mA DC BIAS
 120µH MIN WITH 19mA DC BIAS

INTERWINDING CAPACITANCE, C_{ww}

@1MHz, 20mV
 30pF MAX

PARAMETER		MAGNITUDE (IN dB)	FREQUENCY (IN MHZ)	
			START	END
INSERTION LOSS	SDD12 , SDD21	-0.004<f/MHz>-0.4 MAX	1	150
RETURN LOSS	SDD11 , SDD22	-20 MIN	1	40
		-20+15LOG<f/40MHz> MIN	40	150
ALIEN NEAR END CROSSTALK	SDDXY'	-46+7LOG<f/125MHz> MIN	1	150
NEAR END CROSSTALK	SDDXY	-35 MIN	1	40
		-35+15LOG<f/40MHz> MIN	40	150
MODE CONVERSION	SDC12	-35 MIN	1	40
		-35+17LOG<f/40MHz> MIN	40	150
	SDC21	-30 MIN	1	40
COMMON MODE REJECTION	SCC21	-30+11LOG<f/40MHz> MIN	40	150
		-25 MIN	1	150

BALANCED DC LINE CURRENT

720mA MAX @57VDC CONTINUOUS
 1.2A MAX @57VDC FOR 200MS

HIPOT

1500 V_{rms}

ORIGINATED BY		DATE	TITLE	PART NO. / DRAWING NO.	STANDARD DIM.		[] METRIC DIM. AS REF.		REV. : B	PAGE : 2		
Alice Pang		2018-02-26			ELECTRICAL SPECIFICATION	S558-5500-JD	TOL. IN INCH		UNIT : INCH [mm]			
DRAWN BY		DATE	FILE NAME				.X		SCALE : N/A			
ZC Guo		2018-02-26	S5585500JDB.DWG				.XX		SIZE : A4			
							.XXX					