HDMI Intel® FPGA IP User Guide

Updated for Intel® Quartus® Prime Design Suite: **19.1**

Subscribe
Send Feedback

UG-HDMI | 2019.04.29
Latest document on the web: **PDF** | **HTML**

Contents

1. HDMI Intel® FPGA IP Quick Reference....4

2. HDMI Overview....6
2.1. Device Family Support....10
2.2. Resource Utilization....11

3. HDMI Intel FPGA IP Getting Started....13
3.1. Installing and Licensing Intel FPGA IP Cores....13
3.1.1. Intel FPGA IP Evaluation Mode....14
3.2. Specifying IP Core Parameters and Options....16

4. HDMI Hardware Design Examples....17
4.1. HDMI Hardware Design Examples for Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10 Devices....17
4.2. HDMI Hardware Design Examples for Arria V and Stratix V Devices....17
4.2.1. HDMI Hardware Design Components....17
4.2.2. HDMI Hardware Design Requirements....33
4.2.3. Design Walkthrough....34

5. HDMI Source....38
5.1. Source Functional Description....38
5.1.1. Source Scrambler, TMDS/TERC4 Encoder....39
5.1.2. Source Video Resampler....39
5.1.3. Source Window of Opportunity Generator....41
5.1.4. Source Auxiliary Packet Encoder....42
5.1.5. Source Auxiliary Packet Generators....44
5.1.6. Source Auxiliary Data Path Multiplexers....44
5.1.7. Source Auxiliary Control Port....44
5.1.8. Source Audio Encoder....47
5.2. Source Interfaces....53
5.3. Source Clock Tree....58

6. HDMI Sink....61
6.1. Sink Functional Description....61
6.1.1. Sink Word Alignment and Channel Deskew....61
6.1.2. Sink Descrambler, TMDS/TERC4 Decoder....63
6.1.3. Sink Video Resampler....64
6.1.4. Sink Auxiliary Decoder....64
6.1.5. Sink Auxiliary Packet Capture....66
6.1.6. Sink Auxiliary Data Port....66
6.1.7. Sink Audio Decoder....68
6.1.8. Status and Control Data Channel (SCDC) Interface....68
6.2. Sink Interfaces....69
6.3. Sink Clock Tree....74

7. HDMI Parameters....77
7.1. HDMI Source Parameters....77
7.2. HDMI Sink Parameters....77

8. HDMI Simulation Example.....79
8.1. Simulation Walkthrough.....80
9. HDMI Intel FPGA IP User Guide Archives.....83
10. Document Revision History for the HDMI Intel FPGA IP User Guide.....84

1. HDMI Intel® FPGA IP Quick Reference

The Intel® FPGA High-Definition Multimedia Interface (HDMI) IP core provides support for next-generation video display interface technology. The HDMI Intel FPGA IP core is part of the Intel FPGA IP Library, which is distributed with the Intel Quartus® Prime software.

Information		Description
Release Information	Version	19.1
	Release	April 2019
	Ordering Code	IP-HDMI
IP Core Information	Core Features	• Conforms to the *High-Definition Multimedia Interface (HDMI) Specification versions 1.4 and 2.0b* • Supports transmitter and receiver on a single device transceiver quad • Supports pixel frequency up to 600 MHz • Supports RGB and YCbCr 444, 422, and 420 color modes • Accepts standard H-SYNC, V-SYNC, data enable, RGB video format, and YCbCr video format • Supports up to 32 audio channels in 2-channel and 8-channel layouts. • Supports 1, 2, or 4 symbols per clock • Supports 8, 10, 12, or 16 bits per component (bpc) • Supports single link Digital Visual Interface (DVI) • Supports High Dynamic Range (HDR) InfoFrame insertion and filter through the provided design examples • Supports up to 1,536 kHz audio sample frequency
	Typical Application	• Interfaces within a PC and monitor • External display connections, including interfaces between a PC and monitor or projector, between a PC and TV, or between a device such as a DVD player and TV display
	Device Family	Supports Intel Stratix® 10 (H-tile and L-tile), Intel Arria® 10, Intel Cyclone® 10 GX, Arria V, and Stratix V FPGA devices
	Design Tools	• Intel Quartus Prime software for IP design instantiation and compilation • Timing Analyzer in the Intel Quartus Prime software for timing analysis • ModelSim* - Intel FPGA Edition or ModelSim - Intel FPGA Starter Edition, NCSim, Riviera-PRO*, VCS*, VCS MX, and Xcelium* Parallel software for design simulation

Related Information

- HDMI Intel Arria 10 FPGA IP Design Example User Guide
  For more information about the Intel Arria 10 design examples.

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

- HDMI Intel Cyclone 10 GX FPGA IP Design Example User Guide
  For more information about the Intel Cyclone 10 GX design examples.
- HDMI Intel Stratix 10 FPGA IP Design Example User Guide
  For more information about the Intel Stratix 10 design examples.
- HDMI Intel FPGA IP User Guide Archives on page 83
  Provides a list of user guides for previous versions of the HDMI Intel FPGA IP.

2. HDMI Overview

The HDMI Intel FPGA IP core provides support for next generation video display interface technology.

The HDMI standard specifies a digital communications interface for use in both internal and external connections:

- Internal connections—interface within a PC and monitor
- External display connections—interface between a PC and monitor or projector, between a PC and TV, or between a device such a DVD player and TV display.

The HDMI system architecture consists of sinks and sources. A device may have one or more HDMI inputs and outputs.

The HDMI cable and connectors carry four differential pairs that make up the Transition Minimized Differential Signaling (TMDS) data and clock channels. You can use these channels to carry video, audio, and auxiliary data.

The HDMI also carries a Video Electronics Standards Association (VESA) Display Data Channel (DDC) and Status and Control Data Channel (SCDC). The DDC configures and exchanges status between a single source and a single sink. The source uses the DDC to read the sink's Enhanced Extended Display Identification Data (E-EDID) to discover the sink's configuration and capabilities.

The optional Consumer Electronics Control (CEC) protocol provides high-level control functions between various audio visual products in your environment.

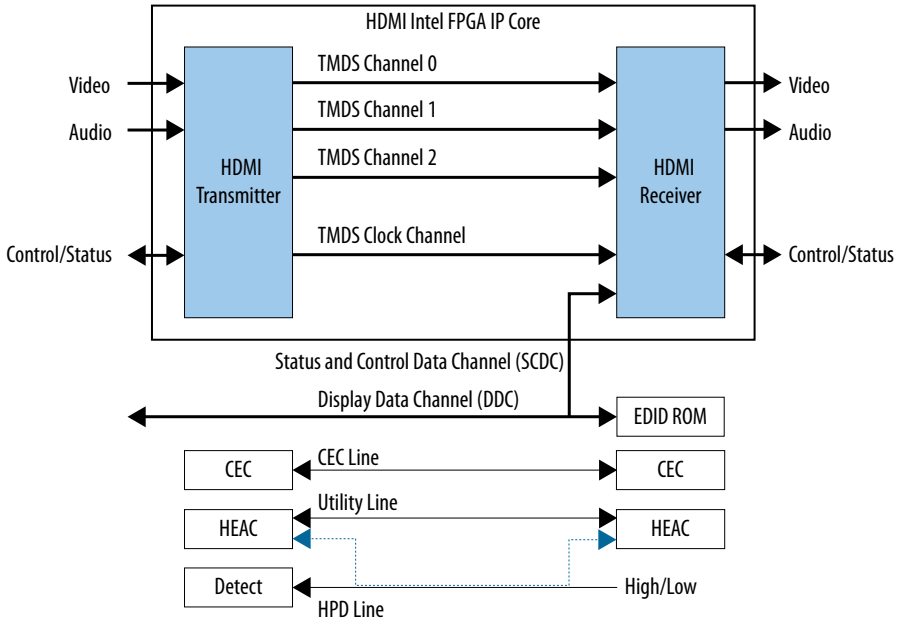
The optional HDMI Ethernet and Audio Return Channel (HEAC) provides Ethernet compatible data networking between connected devices and an audio return channel in the opposite direction of TMDS. The HEAC also uses Hot-Plug Detect (HPD) line for signal transmission.

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

Figure 1. HDMI Intel FPGA Core Block Diagram

The figure below illustrates the blocks in the HDMI Intel FPGA IP core.



Based on TMDS encoding, the HDMI protocol allows the transmission of both audio and video data between source and sink devices.

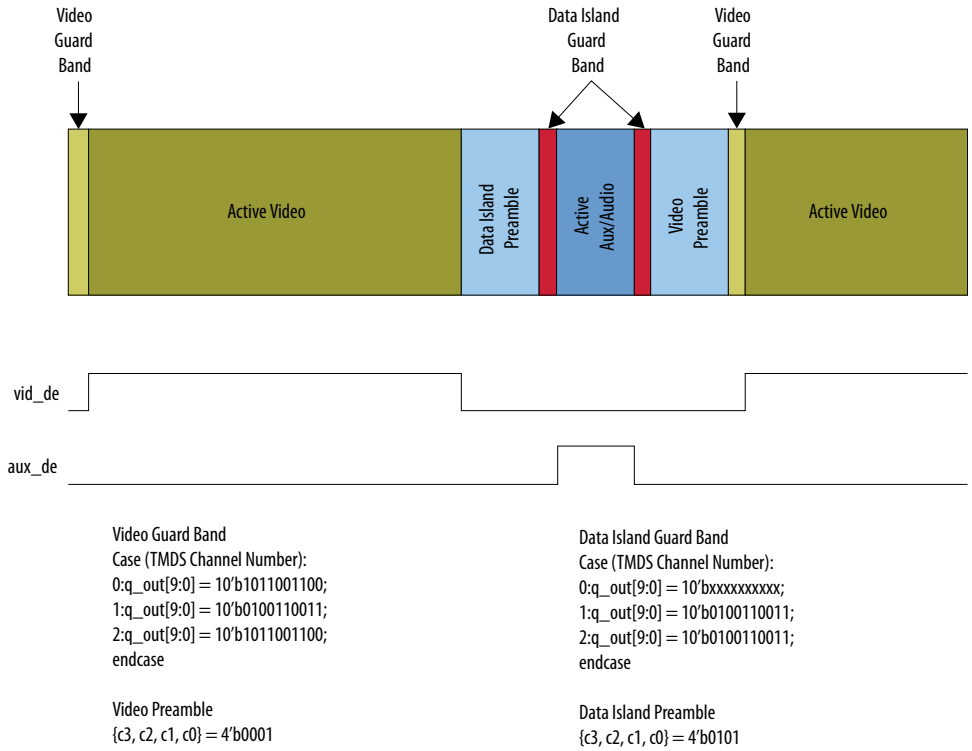
An HDMI interface consists of three color channels accompanied by a single clock channel. You can use each color line to transfer both individual RGB colors and auxiliary data.

Note: Refer to *AN 837: Design Guidelines for Intel FPGA HDMI* to know more about the channel mapping to the RGB colors.

The receiver uses the TMDS clock as a frequency reference for data recovery on the three TMDS data channels. This clock typically runs at the video pixel rate.

TMDS encoding is based on an 8-bit to 10-bit algorithm. This protocol attempts to minimize data channel transition, and yet maintain sufficient transition so that a sink device can lock reliably to the data stream.

Figure 2. HDMI Intel FPGA Video Stream Data



The figure above illustrates two data streams:

- Data stream in green—transports color data
- Data stream in dark blue—transports auxiliary data

Table 1. Video Data and Auxiliary Data

The table below describes the function of the video data and auxiliary data.

Data	Description
Video data	• Packed representation of the video pixels clocked at the source pixel clock. • Encoded using the TMDS 8-bit to 10-bit algorithm.
Auxiliary data	• Transfers audio data together with a range of auxiliary data packets. • Sink devices use auxiliary data packets to correctly reconstruct video and audio data. • Encoded using the TMDS Error Reduction Coding–4 bits (TERC4) encoding algorithm.

Each data stream section is preceded with guard bands and pre-ambles. The guard bands and pre-ambles allow for accurate synchronization with received data streams.

The following figures show the arrangement of the video data, video data enable, video H-SYNC, and video V-SYNC in 1, 2, and 4 symbols per clock.

Figure 3. Video Data, Video Data Valid, H-SYNC, and V-SYNC—1 Symbol per Clock

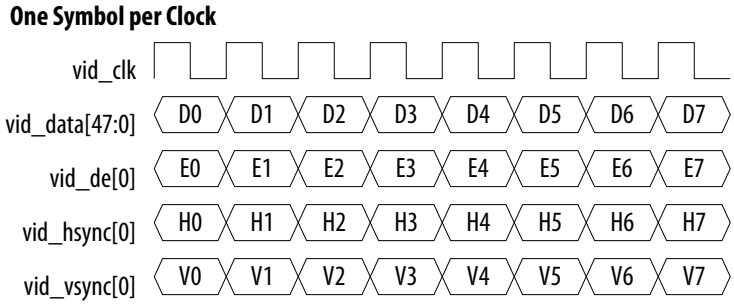


Figure 4. Video Data, Video Data Valid, H-SYNC, and V-SYNC—2 Symbols per Clock

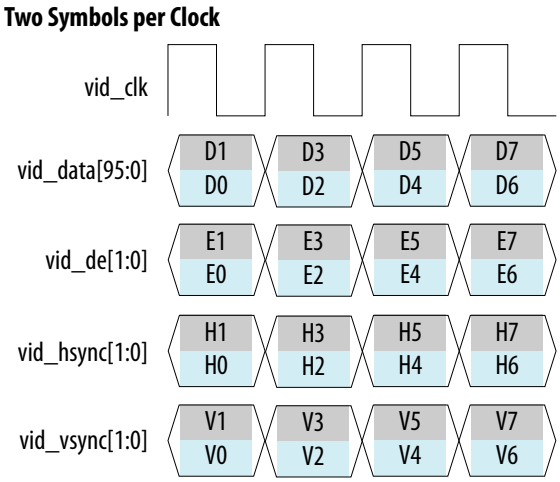
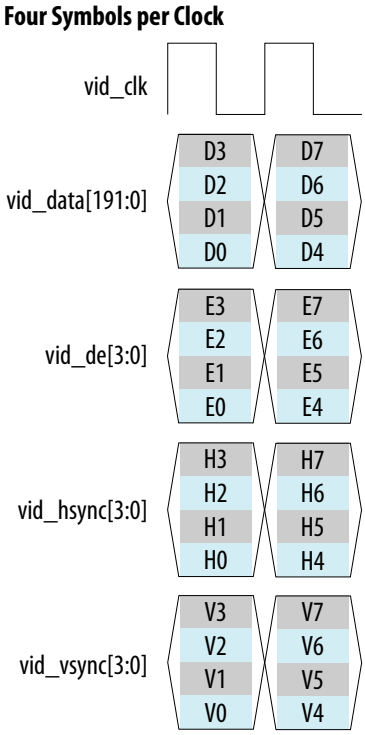


Figure 5. Video Data, Video Data Valid, H-SYNC, and V-SYNC—4 Symbols per Clock



Related Information

AN 837: Design Guidelines for Intel FPGA HDMI

2.1. Device Family Support

Table 2. Intel Device Family Support

Device Family	Support Level
Intel Stratix 10 (H-tile and L-tile)	Final
Intel Arria 10	Final
Intel Cyclone 10 GX	Final
Arria V	Final
Stratix V	Final

The following terms define device support levels for Intel FPGA IP cores:

- Advance support—the IP core is available for simulation and compilation for this device family. Timing models include initial engineering estimates of delays based on early post-layout information. The timing models are subject to change as silicon testing improves the correlation between the actual silicon and the timing models. You can use this IP core for system architecture and resource utilization studies, simulation, pinout, system latency assessments, basic timing assessments (pipeline budgeting), and I/O transfer strategy (data-path width, burst depth, I/O standards tradeoffs).
- Preliminary support—the IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution.
- Final support—the IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

2.2. Resource Utilization

The resource utilization data indicates typical expected performance for the HDMI Intel FPGA IP core.

Table 3. HDMI Data Rate

The table lists the maximum data rates for HDMI Intel FPGA IP core configurations of 1, 2, and 4 symbols per clock.

Devices	Maximum Data Rate (Mbps)		
	1 Symbol per Clock	2 Symbols per Clock	4 Symbols per Clock
Intel Stratix 10	Not Supported	5,940 (Example: 4Kp60 8 bpc)	Not Supported
Intel Arria 10	Not Supported	5,940 (Example: 4Kp60 8 bpc)	Not Supported
Intel Cyclone 10 GX	Not Supported	5,940 (Example: 4Kp60 8 bpc)	Not Supported
Arria V GX	1,875 (Example: 1080p60 10 bpc)	3,276.8 (Example: 4Kp30 8 bpc)	5,940 (Example: 4Kp60 8 bpc)
Stratix V	2,970 (Example: 4Kp30 8 bpc)	5,940 (Example: 4Kp60 8 bpc)	Not Supported

Table 4. Color Depth Supported for Each Pixel Encoding

Pixel Encoding	Color Depth			
	8	10	12	16
RGB	Yes	Yes	Yes	Yes
YCbCr 4:4:4	Yes	Yes	Yes	Yes
YCbCr 4:2:2(1)	Yes	Yes	Yes	Not applicable
YCbCr 4:2:0	Yes	Yes	Yes	Yes

Table 5. HDMI Intel FPGA Resource Utilization

The table lists the performance data for the different Intel FPGA devices.

Device	Symbols per Clock	Direction	ALMs	Logic Registers		Memory	
				Primary	Secondary	Bits	M10K or M20K
Intel Stratix 10 H-tile	2	RX	5.041	6,633	902	38,400	14
	2	TX	4,975	7,559	1,368	37,568	13
Intel Stratix 10 L-tile	2	RX	5,025	6,584	967	38,400	14
	2	TX	4,966	7,539	1,425	37,568	13
Intel Arria 10	2	RX	3,952	5,716	1,049	38,400	14
	2	TX	4,422	7,016	1,701	36,968	13
Intel Cyclone 10 GX	2	RX	4,000	5,768	965	38,400	14
	2	TX	4,484	7,167	1,629	36,968	13
Arria V GX	1	RX	2,630	4,039	402	35,712	13
	1	TX	2,700	4,462	417	11,108	11
	2	RX	3,446	4,656	531	38,400	14
	2	TX	3,759	6,091	450	12,680	13
	4	RX	4,895	5,937	614	43,776	20
	4	TX	6,135	9,156	445	15,824	18
Stratix V	1	RX	2,592	3,946	398	35,712	13
	1	TX	2,634	4,415	461	11,108	11
	2	RX	3,337	4,619	440	38,400	14
	2	TX	3,644	5,919	680	12,680	13

Table 6. Recommended Speed Grades for Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX Devices

Device	Lane Rate (Mbps)	Interface Width (bits)	Speed Grades
Intel Stratix 10	6,000	20	-1, -2
Intel Arria 10	6,000	20	-1, -2
Intel Cyclone 10 GX	6,000	20	-5

(1) According to *HDMI 1.4b Specification Section 6.5.1*, 8 and 10 bpc use the same pixel encoding as 12 bpc, but the valid bits are left-justified with zeros padding the bits below the least significant bit.

3. HDMI Intel FPGA IP Getting Started

This chapter provides a general overview of the Intel IP core design flow to help you quickly get started with the HDMI Intel FPGA IP core. The Intel FPGA IP Library is installed as part of the Intel Quartus Prime installation process. You can select and parameterize any Intel FPGA IP core from the library. Intel provides an integrated parameter editor that allows you to customize the HDMI Intel FPGA IP core to support a wide variety of applications. The parameter editor guides you through the setting of parameter values and selection of optional ports.

Related Information

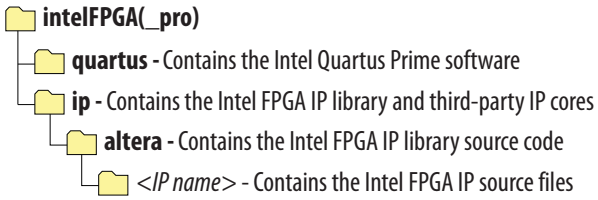
- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Creating Version-Independent IP and Platform Designer Simulation Scripts
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.

3.1. Installing and Licensing Intel FPGA IP Cores

The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production.

The Intel Quartus Prime software installs IP cores in the following locations by default:

Figure 6. IP Core Installation Path



Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

Table 7. IP Core Installation Locations

Location	Software	Platform
`<drive>:\intelFPGA_pro\quartus\ip\altera`	Intel Quartus Prime Pro Edition	Windows*
`<drive>:\intelFPGA\quartus\ip\altera`	Intel Quartus Prime Standard Edition	Windows
`<home directory>:/intelFPGA_pro/quartus/ip/altera`	Intel Quartus Prime Pro Edition	Linux*
`<home directory>:/intelFPGA/quartus/ip/altera`	Intel Quartus Prime Standard Edition	Linux

Note: The Intel Quartus Prime software does not support spaces in the installation path.

3.1.1. Intel FPGA IP Evaluation Mode

The free Intel FPGA IP Evaluation Mode allows you to evaluate licensed Intel FPGA IP cores in simulation and hardware before purchase. Intel FPGA IP Evaluation Mode supports the following evaluations without additional license:

- Simulate the behavior of a licensed Intel FPGA IP core in your system.
- Verify the functionality, size, and speed of the IP core quickly and easily.
- Generate time-limited device programming files for designs that include IP cores.
- Program a device with your IP core and verify your design in hardware.

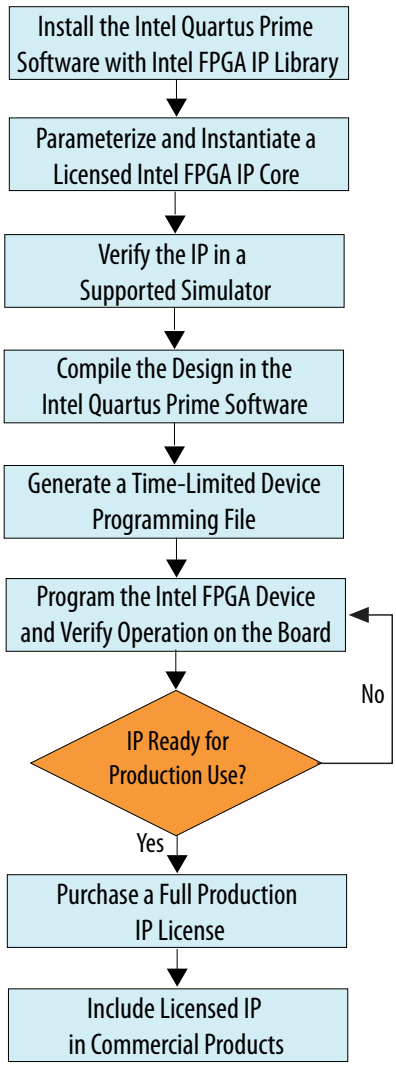
Intel FPGA IP Evaluation Mode supports the following operation modes:

- **Tethered**—Allows running the design containing the licensed Intel FPGA IP indefinitely with a connection between your board and the host computer. Tethered mode requires a serial joint test action group (JTAG) cable connected between the JTAG port on your board and the host computer, which is running the Intel Quartus Prime Programmer for the duration of the hardware evaluation period. The Programmer only requires a minimum installation of the Intel Quartus Prime software, and requires no Intel Quartus Prime license. The host computer controls the evaluation time by sending a periodic signal to the device via the JTAG port. If all licensed IP cores in the design support tethered mode, the evaluation time runs until any IP core evaluation expires. If all of the IP cores support unlimited evaluation time, the device does not time-out.
- **Untethered**—Allows running the design containing the licensed IP for a limited time. The IP core reverts to untethered mode if the device disconnects from the host computer running the Intel Quartus Prime software. The IP core also reverts to untethered mode if any other licensed IP core in the design does not support tethered mode.

When the evaluation time expires for any licensed Intel FPGA IP in the design, the design stops functioning. All IP cores that use the Intel FPGA IP Evaluation Mode time out simultaneously when any IP core in the design times out. When the evaluation time expires, you must reprogram the FPGA device before continuing hardware verification. To extend use of the IP core for production, purchase a full production license for the IP core.

You must purchase the license and generate a full production license key before you can generate an unrestricted device programming file. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (`<project name>_time_limited.sof`) that expires at the time limit.

Figure 7. Intel FPGA IP Evaluation Mode Flow



Note: Refer to each IP core's user guide for parameterization steps and implementation details.

Intel licenses IP cores on a per-seat, perpetual basis. The license fee includes first-year maintenance and support. You must renew the maintenance contract to receive updates, bug fixes, and technical support beyond the first year. You must purchase a full production license for Intel FPGA IP cores that require a production license, before generating programming files that you may use for an unlimited time. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (`<project name>_time_limited.sof`) that expires at the time limit. To obtain your production license keys, visit the Self-Service Licensing Center.

The Intel FPGA Software License Agreements govern the installation and use of licensed IP cores, the Intel Quartus Prime design software, and all unlicensed IP cores.

Related Information

- Intel Quartus Prime Licensing Site
- Introduction to Intel FPGA Software Installation and Licensing

3.2. Specifying IP Core Parameters and Options

Follow these steps to specify the HDMI Intel FPGA IP core parameters and options.

1. Create a Intel Quartus Prime project using the **New Project Wizard** available from the File menu.
2. On the **Tools** menu, click **IP Catalog**.
3. Under **Installed IP**, double-click **Library ➤ Interface ➤ Protocols ➤ Audio&Video ➤ HDMI Intel FPGA**.
   The parameter editor appears.
4. Specify a top-level name for your custom IP variation. This name identifies the IP core variation files in your project. If prompted, also specify the targeted FPGA device family and output file HDL preference. Click **OK**.
5. Specify parameters and options in the HDMI parameter editor:
   - Optionally select preset parameter values. Presets specify all initial parameter values for specific applications (where provided).
   - Specify parameters defining the IP core functionality, port configurations, and device-specific features.
   - Specify options for generation of a timing netlist, simulation model, testbench, or example design (where applicable).
   - Specify options for processing the IP core files in other EDA tools.
6. Click **Generate** to generate the IP core and supporting files, including simulation models.
7. Click **Close** when file generation completes.
8. Click **Finish**.
9. If you generate the HDMI Intel FPGA IP core instance in a Intel Quartus Prime project, you are prompted to add `Intel Quartus Prime IP File (.qip)` and `Intel Quartus Prime Simulation IP File (.sip)` to the current Intel Quartus Prime project.

4. HDMI Hardware Design Examples

Intel offers design examples that you can simulate, compile, and test in hardware.

The implementation of the HDMI Intel FPGA IP on hardware requires additional components specific to the targeted device.

4.1. HDMI Hardware Design Examples for Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10 Devices

The HDMI Intel FPGA IP core offers design examples that you can generate through the IP catalog in the Intel Quartus Prime Pro Edition software.

Related Information

- HDMI Intel Arria 10 FPGA IP Design Example User Guide
  For more information about the Intel Arria 10 design examples.
- HDMI Intel Cyclone 10 GX FPGA IP Design Example User Guide
  For more information about the Intel Cyclone 10 GX design examples.
- HDMI Intel Stratix 10 FPGA IP Design Example User Guide
  For more information about the Intel Stratix 10 design examples.

4.2. HDMI Hardware Design Examples for Arria V and Stratix V Devices

The HDMI hardware design example helps you evaluate the functionality of the HDMI Intel FPGA IP core and provides a starting point for you to create your own design for Arria V and Stratix V devices.

The design example runs on the following device kits:

- Arria V GX starter kit
- Stratix V GX development kit
- Bitec HDMI HSMC 2.0 Daughter Card Revision 8

Related Information

AN 837: Design Guidelines for Intel FPGA HDMI

4.2.1. HDMI Hardware Design Components

The demonstration designs instantiate the Video and Image Processing (VIP) Suite IP cores or FIFO buffers to perform a direct HDMI video stream passthrough between the HDMI sink and source.

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

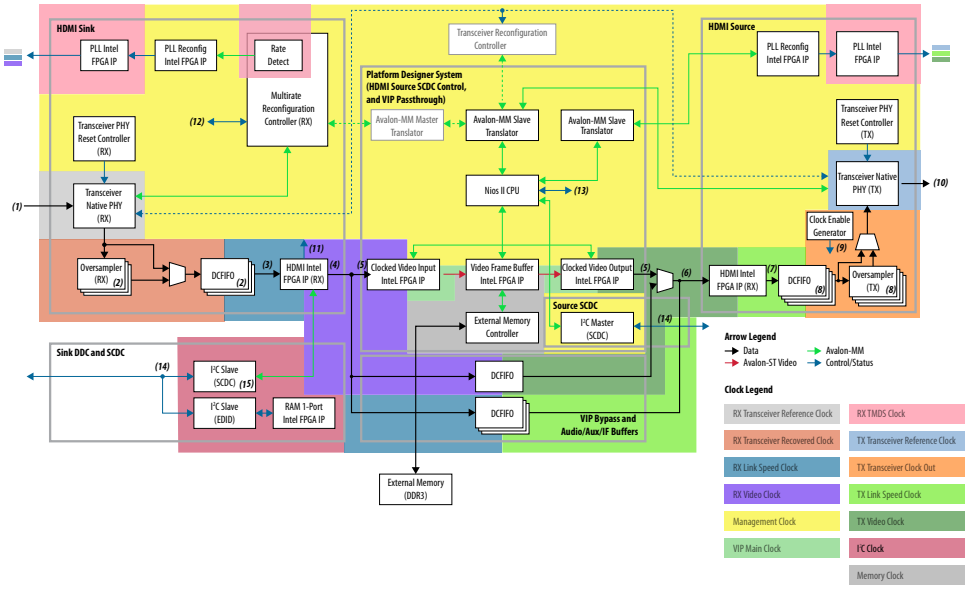
ISO 9001:2015 Registered

The hardware demonstration design comprises the following components:

- HDMI sink
  - Transceiver Native PHY (RX)
  - Transceiver PHY Reset Controller (RX)
  - PLL
  - PLL Reconfiguration
  - Multirate Reconfiguration Controller (RX)
  - Oversampler (RX)
  - DCFIFO
- Sink Display Data Channel (DDC) and Status and Control Data Channel (SCDC)
- Transceiver Reconfiguration Controller
- VIP bypass and Audio, Auxiliary and InfoFrame buffers
- Platform Designer system
  - VIP passthrough for HDMI video stream
  - Source SCDC controller
  - HDMI source reconfiguration controller
- HDMI source
  - Transceiver Native PHY (TX)
  - Transceiver fPLL
  - Transceiver PHY Reset Controller (TX)
  - PLL
  - PLL Reconfiguration
  - Oversampler (TX)
  - DCFIFO
  - Clock Enable Generator

Figure 8. HDMI Hardware Design Example Block Diagram

The figure below shows a high level architecture of the design.



The following details of the design example architecture correspond to the numbers in the block diagram.

1. The sink TMDS data has three channels: data channel 0 (blue), data channel 1 (green), and data channel 2 (red).
2. The Oversampler (RX) and dual-clock FIFO (DCFIFO) instances are duplicated for each TMDS data channel (0,1,2).
3. The video data input width for each color channel of the HDMI RX core is equivalent to RX transceiver PCS-PLD parallel data width per channel.
4. Each color channel is fixed at 16 bpc. The video data output width of the HDMI RX core is equivalent to the value of symbols per clock*16*3.
5. The video data input width of the Clocked Video Input (CVI) and Clocked Video Output (CVO) IP cores are equivalent to the value of NUMBER_OF_PIXELS_IN_PARALLEL * BITS_PER_PIXEL_PER_COLOR_PLANE * NUMBER_OF_COLOR_PLANES. To interface with the HDMI core, the values of NUMBER_OF_PIXELS_IN_PARALLEL, BITS_PER_PIXEL_PER_COLOR_PLANE, and NUMBER_OF_COLOR_PLANES must match the symbols per clock, 16 and 3 respectively.
6. The video data input width of the HDMI TX core is equivalent to the value of symbols per clock*16*3. You can use the user switch to select the video data from the CVO IP core (VIP passthrough) or DCFIFO (VIP bypass).
7. The video data output width for each color channel of the HDMI TX core is equivalent to TX transceiver PCS-PLD parallel data width per channel.
8. The DCFIFO and the Oversampler (TX) instances are duplicated for each TMDS data channel (0,1,2) and clock channel.
9. The Oversampler (TX) uses the clock enable signal to read data from the DCFIFO.
10. The source TMDS data has four channels: data channel 0 (blue), data channel 1 (green), data channel 2 (red), and clock channel.

11. The RX Multirate Reconfiguration Controller requires the status of `TMDS_Bit_clock_Ratio` port to perform appropriate RX reconfiguration between the TMDS character rates below 340 Mcsc (HDMI 1.4b) and above 340 Mcsc (HDMI 2.0b). The status of the port is also required by the Nios II processor and the HDMI TX core to perform appropriate TX reconfiguration and scrambling.
12. The reset control and lock status signals from HDMI PLL, RX Transceiver Reset Controller and HDMI RX core.
13. The reset and oversampling control signals for HDMI PLL, TX Transceiver Reset Controller, and HDMI TX core. The lock status and rate detection measure valid signals from the HDMI sink initiate the TX reconfiguration process.
14. The I^2C SCL and SDA lines with tristate buffer for bidirectional configuration. Use the ALTIOBUF IP core for Arria V and Stratix V devices.
15. The SCDC is mainly designed for the source to update the `TMDS_Bit_Clock_Ratio` and `Scrambler_Enable` bits of the sink TMDS Configuration register. .

4.2.1.1. Transceiver Native PHY (RX)

- Transceiver Native PHY in Arria V devices
  - To operate the TMDS bit rate up to 3,400 Mbps, configure the Transceiver Native PHY at 20 bits at PCS – PLD interface with the HDMI RX core at 2 symbols per clock. When the PCS – PLD interface width is 20 bits, the minimum link rate is 611 Mbps.
  - To operate the TMDS bit rate up to 6,000 Mbps, configure the Transceiver Native PHY at 40 bits with the HDMI RX core at 4 symbols per clock. When the PCS – PLD interface width is 40 bits, the minimum link rate is 1,000 Mbps.
  - Oversampling is required for TMDS bit rate which is below the minimum link rate.
- Transceiver Native PHY in Stratix V devices
  - To operate the TMDS bit rate up to 6,000 Mbps, configure the Transceiver Native PHY at 20 bits at PCS – PLD interface with the HDMI RX core at 2 symbols per clock. When the PCS – PLD interface width is 20 bits, the minimum link rate is 611 Mbps.

Table 8. Arria V and Stratix V Transceiver Native PHY (RX) Configuration Settings (6,000 Mbps)

This table shows an example of Arria V and Stratix V Transceiver Native PHY (RX) configuration settings for TMDS bit rate of 6,000 Mbps.

Parameters	Settings
Datapath Options	
Enable TX datapath	Off
Enable RX datapath	On
Enable Standard PCS	On
Initial PCS datapath selection	Standard
Number of data channels	3
Enable simplified data interface	On

RX PMA	
Data rate	6,000 Mbps
Enable CDR dynamic reconfiguration	On
Number of CDR reference clocks	2 [(2)]
Selected CDR reference clock	0 [(2)]
Selected CDR reference clock frequency	600 MHz
PPM detector threshold	1,000 PPM
Enable rx_pma_clkout port	On
Enable rx_is_lockedtodata port	On
Enable rx_is_lockedtoref port	On
Enable rx_set_locktodata and rx_set_locktoref ports	On

Standard PCS	
Standard PCS protocol	Basic
Standard PCS/PMA interface width	• 10 (for 1 symbol per clock) • 20 (for 2 and 4 symbols per clock)
Enable RX byte deserializer	• Off (for 1 and 2 symbols per clock) • On (for 4 symbols per clock)

(2) The Bitec HDMI HSMC 2.0 daughter card routes the TMDS clock pin to the transceiver serial data pin. To use the TMDS clock to drive the HDMI PLL, the TMDS clock must also drive the transceiver dedicated reference clock pin. The number of CDR reference clocks is 2 with reference clock 1 (unused) driven by the TMDS clock and reference clock 0 driven by the HDMI PLL output clock. The selected CDR reference clock will be fixed at 0.

Table 9. Arria V and Stratix V Transceiver Native PHY (RX) Common Interface Ports

This table describes the Arria V and Stratix V Transceiver Native PHY (RX) common interface ports.

Signals	Direction	Description
Clocks		
`rx_cdr_refclk[1:0]`	Input	Input reference clock for the RX CDR circuitry. • To support arbitrary wide data rate range from 250 Mbps to 6,000 Mbps, you need a generic core PLL to obtain a higher clock frequency from the TMDS clock. You need a higher clock frequency to create oversampled stream for data rates below the minimum transceiver data rate—for example, 611 Mbps or 1,000 Mbps). • If the TMDS clock pin is routed to the transceiver dedicated reference clock pin, you only need to create one transceiver reference clock input. You can use the TMDS clock as reference clock for a generic core PLL to drive the transceiver. • If you use Bitec HDMI HSMC 2.0 daughter card, the TMDS clock pin is routed to the transceiver serial data pin. In this case, to use the TMDS clock as a reference clock for a generic core PLL, the clock must also drive the transceiver dedicated reference clock. Connect bit 0 to the generic core PLL output and bit 1 to the TMDS clock and set the selected CDR reference clock at 0.
`rx_std_clkout[2:0]`	Output	RX parallel clock output. • The CDR circuitry recovers the RX parallel clock from the RX data stream when the CDR is configured at lock-to-data mode. • The RX parallel clock is a mirror of the CDR reference clock when the CDR is configured at lock-to-reference mode.
`rx_std_coreclkin[2:0]`	Input	RX parallel clock that drives the read side of the RX phase compensation FIFO. Connect to `rx_std_clkout` ports.
`rx_pma_clkout[2:0]`	Output	RX parallel clock (recovered clock) output from PMA. Leave unconnected.
Resets		
`rx_analogreset[2:0]`	Input	Active-high, edge-sensitive, asynchronous reset signal. When asserted, resets the RX CDR circuit, deserializer. Connect to Transceiver PHY Reset Controller IP core.
`rx_digitalreset[2:0]`	Input	Active-high, edge-sensitive, asynchronous reset signal. When asserted, resets the digital component of the RX data path. Connect to the Transceiver PHY Reset Controller IP core.
PMA Ports		
`rx_set_locktoref[2:0]`	Input	When asserted, programs the RX CDR to lock to reference mode manually. The lock to reference mode enables you to control the reset sequence using `rx_set_locktoref` and `rx_set_locktodata`. The Multirate Reconfiguration Controller (RX) sets this port to 1 if oversampling mode is required. Otherwise, this port is set to 0.

continued...

PMA Ports		
		Refer "Transceiver Reset Sequence" in Transceiver Reset Control in Arria V/Stratix V Devices for more information about manual control of the reset sequence.
`rx_set_locktodata[2:0]`	Input	Always driven to 0. When `rx_set_locktoref` is driven to 1, the CDR is configured to `lock-to-reference` mode. Otherwise, the CDR is configured to `lock-to-data` mode.
`rx_is_lockedtoref[2:0]`	Output	When asserted, the CDR is locked to the incoming reference clock. Connect this port to `rx_is_lockedtodata` port of the Transceiver PHY Reset Controller IP core when `rx_set_locktoref` is 1.
`rx_is_lockedtodata[2:0]`	Output	When asserted, the CDR is locked to the incoming data. Connect this port to `rx_is_lockedtodata` port of Transceiver PHY Reset Controller IP core when `rx_set_locktoref` is 0.
`rx_serial_data[2:0]`	Input	RX differential serial input data.

PCS Ports		
`unused_rx_parallel_data`	Output	Leave unconnected.
`rx_parallel_data[S*3*10-1:0]`	Output	PCS RX parallel data. *Note:* S=Symbols per clock.

Calibration Status Port		
`rx_cal_busy[2:0]`	Output	When asserted, indicates that the initial RX calibration is in progress. This port is also asserted if the reconfiguration controller is reset. Connect to the Transceiver PHY Reset Controller IP core.

Reconfiguration Ports		
`reconfig_to_xcvr[209:0]`	Input	Reconfiguration signals from the Transceiver Reconfiguration Controller.
`reconfig_from_xcvr[137:0]`	Output	Reconfiguration signals to the Transceiver Reconfiguration Controller.

4.2.1.2. PLL Intel FPGA IP Cores

Use the PLL Intel FPGA IP core as the HDMI PLL to generate reference clock for RX or TX transceiver, link speed, and video clocks for the HDMI RX or TX IP core.

The HDMI PLL is referenced by the arbitrary TMDS clock. For HDMI source, you can reference the HDMI PLL by a separate clock source in the VIP passthrough design, which contains frame buffer. The HDMI PLL for TX has the same desired output frequencies as RX across symbols per clock and color depth.

- For TMDS bit rates ranging from 3,400 Mbps to 6,000 Mbps (HDMI 2.0), the TMDS clock rate is 1/40 of the TMDS bit rate. The HDMI PLL generates reference clock for RX/TX transceiver at 4 times the TMDS clock.
- For TMDS bit rates below 3,400 Mbps (HDMI 1.4b), the TMDS clock rate is 1/10 of the TMDS bit rate. The HDMI PLL generates reference clock for RX/TX transceiver at identical rate as the TMDS clock.

If the TMDS link operates at TMDS bit rates below the minimum RX/TX transceiver link rate, your design requires oversampling and a factor of 5 is chosen. The minimum link rate of the RX/TX transceiver vary across device families and symbols per clock. The HDMI PLL generates reference clock for RX/TX transceiver at 5 times the TMDS clock.

Note: Place the PLL Intel FPGA block on the transmit path (`pll_hdmi_tx`) in the physical location next to the transceiver PLL.

Table 10. HDMI PLL Desired Output Frequencies for 8-bpc Video

This table shows an example of HDMI PLL desired output frequencies across various TMDS clock rates and symbols per clock for all supported device families using 8-bpc video.

Device Family	Symbols Per Clock	Minimum Link Rate (Mbps)	TMDS Bit Rate (Mbps)	Oversampling (5x) Required	TMDS Clock Rate (MHz)	RX/TX Transceiver Refclk (MHz)	RX/TX Link Speed Clock (MHz)	RX/TX Video Clock (MHz)
Arria V	2	611	270	Yes	27	135	13.5	13.5
			742.5	No	74.25	74.25	37.125	37.125
			1,485	No	148.5	148.5	74.25	74.25
			2,970	No	297	297	148.5	148.5
	4	1,000	270	Yes	27	135	6.75	6.75
			742.5	Yes	74.25	371.25	18.5625	18.5625
			1,485	No	148.5	148.5	37.125	37.125
			5,940	No	148.5	594	148.5	148.5
Stratix V	2	611	540	Yes	54	270	27	27
			1,620	No	162	162	81	81
			5,934	No	296.7	593.4	296.7	296.7

The color depths greater than 8 bpc or 24 bpp are defined to be deep color. For a color depth of 8 bpc, the core carries the pixels at a rate of one pixel per TMDS clock. At deeper color depths, the TMDS clock runs faster than the source pixel clock to provide the extra bandwidth for the additional bits.

The TMDS clock rate is increased by the ratio of the pixel size to 8 bits:

- 8 bits mode—TMDS clock = 1.0 × pixel or video clock (1:1)
- 10 bits mode—TMDS clock = 1.25 × pixel or video clock (5:4)
- 12 bits mode—TMDS clock = 1.5 × pixel or video clock (3:2)
- 16 bits mode—TMDS clock = 2 × pixel or video clock (2:1)

Table 11. HDMI PLL Desired Output Frequencies for Deep Color Video

This table shows an example of HDMI PLL desired output frequencies across symbols per clock and color depths.

Symbols Per Clock	Oversampling (5x) Required	Bits Per Component	TMDS Bit Rate (Mbps)	TMDS Clock Rate (MHz)	RX/TX Transceiver Refclk (MHz)	RX/TX Link Speed Clock (MHz)	RX/TX Video Clock (MHz)
2	Yes	8	270	27	135	13.5	13.5
		10 [3]	337.5	33.75	168.75	16.875	13.5

continued...

Symbols Per Clock	Oversampling (5x) Required	Bits Per Component	TMDS Bit Rate (Mbps)	TMDS Clock Rate (MHz)	RX/TX Transceiver Refclk (MHz)	RX/TX Link Speed Clock (MHz)	RX/TX Video Clock (MHz)
		12 (3)	405	40.5	202.5	20.25	13.5
		16 (3)	540	54	270	27	13.5
4	No	8	1,485	148.5	148.5	37.125	37.125
		10 (3)	1,856.25	185.625	185.625	46.40625	37.125
		12 (3)	2,227.5	222.75	222.75	55.6875	37.125
		16 (3)	2,970	297	297	74.25	37.125

The default frequency setting of the HDMI PLL is fixed at possible maximum value for each clock for appropriate timing analysis.

Note: This default combination is not valid for any HDMI resolution. The core will reconfigure to the appropriate settings upon power up.

4.2.1.3. PLL Reconfig Intel FPGA IP Core

The PLL Reconfig Intel FPGA IP core facilitates dynamic real-time reconfiguration of PLLs in Intel FPGAs.

Use the IP core to update the output clock frequency, PLL bandwidth in real-time, without reconfiguring the entire FPGA.

You can run this IP core at 100 MHz in Stratix V devices. In Arria V devices, you need to run at 75 MHz for timing closure. To simplify clocking in Arria V devices, the entire management clock domain is capped at 75 MHz.

4.2.1.4. Multirate Reconfig Controller (RX)

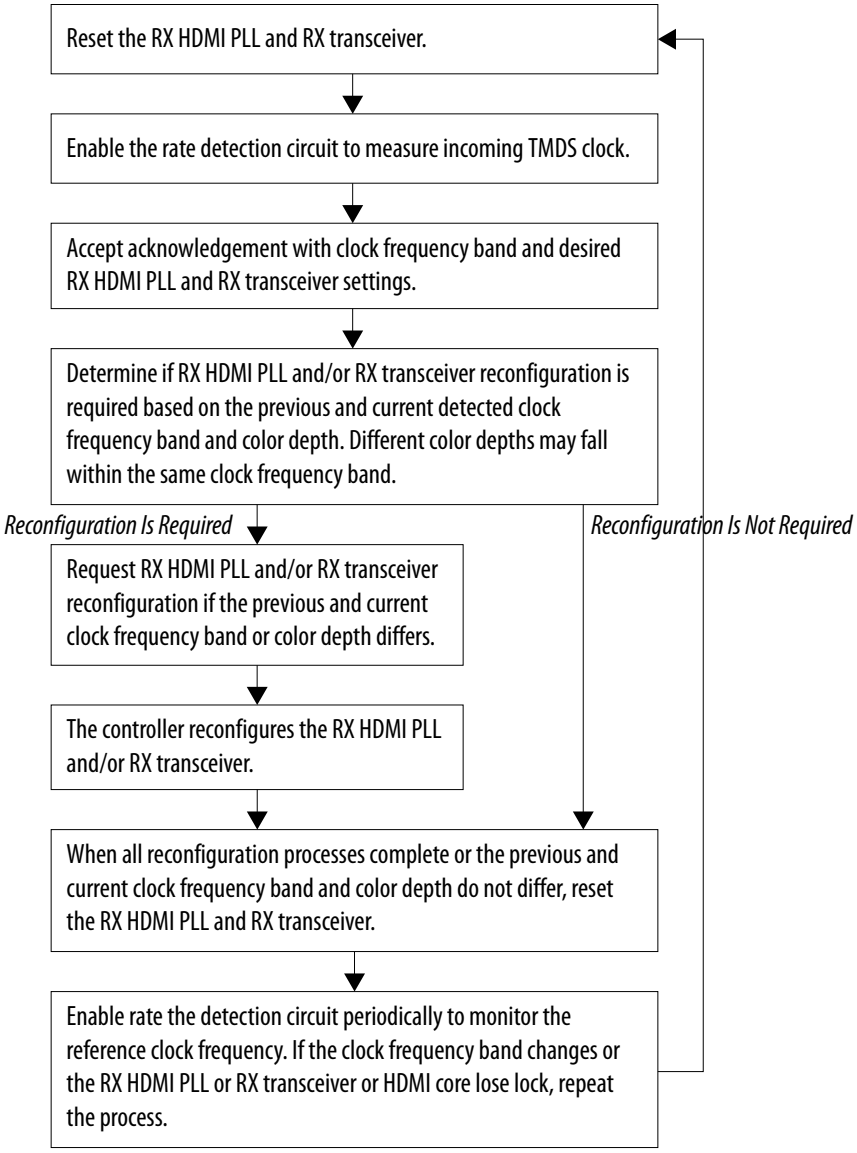
The Multirate Reconfig Controller implements rate detection circuitry with the HDMI PLL to drive the RX transceiver to operate at any arbitrary link rates ranging from 250 Mbps to 6,000 Mbps. Link rate of 6,000 Mbps is not the absolute maximum but the intention is to support HDMI 2.0b link rate.

The Multirate Reconfig Controller performs rate detection on the HDMI PLL arbitrary reference clock, which is also the TMDS clock, to determine the clock frequency band. Based on the detected clock frequency band, the circuitry dynamically reconfigures the HDMI PLL and transceiver settings to accommodate for the link rate change.

(3) For this release, deep color video is only demonstrated in VIP bypass mode. It is not available in VIP passthrough mode.

Figure 9. Multirate Reconfiguration Sequence Flow

This figure illustrates the multirate reconfiguration sequence flow of the controller when it receives input data stream and reference clock frequency, or when the transceiver is unlocked.



4.2.1.5. Oversampler (RX)

The Oversampler (RX) extracts data from the oversampled incoming data stream when the detected clock frequency band is below the transceiver minimum link rate.

The oversampling factor is fixed at 5 and you can program the data width to support different number of symbols. The supported data width is 20 bit for 2 symbols per clock and 40 bits for 4 symbols per clock. The extracted bit will be accompanied by data valid pulse which asserts every 5 clock cycles.

4.2.1.6. DCFIFO

The DCFIFO transfers data from the RX transceiver recovered clock domain to the RX link speed clock domain. The DCFIFO transfers data from the TX link speed clock domain to the TX transceiver parallel clock out domain.

- Sink
  - When the Multirate Reconfig Controller (RX) detects an incoming input stream that is below the transceiver minimum link rate, the DCFIFO accepts the data from the Oversampler with data valid pulse as write request asserted every 5 clock cycles.
  - Otherwise, it accepts data directly from the transceiver with write request asserted at all times.
- Source
  - When Nios II processor determines the outgoing data stream is below the TX transceiver minimum link rate, the TX transceiver accepts the data from the Oversampler (TX).
  - Otherwise, the TX transceiver reads data directly from the DCFIFO with read request asserted at all times.

4.2.1.7. Sink Display Data Channel (DDC) & Status and Control Data Channel (SCDC)

The HDMI source uses the DDC to determine the capabilities and characteristics of the sink by reading the Enhanced Extended Display Identification Data (E-EDID) data structure.

The E-EDID memory is stored using the RAM 1-Port IP core. A standard two-wire (clock and data) serial data bus protocol (I2C slave-only controller) is used to transfer CEA-861-D compliant E-EDID data structure.

The 8-bit I^2C slave addresses for the E-EDID are 0xA0/0xA1. The LSB indicates the access type: 1 for read and 0 for write. When an HPD event occurs, the I^2C slave responds to E-EDID data by reading from the RAM.

The I^2C slave-only controller is also used to support SCDC for HDMI 2.0b operation. The 8-bit I^2C slave addresses for the SCDC are 0xA8/0xA9. When an HPD event occurs, the I^2C slave performs write/read transaction to/from SCDC interface of HDMI RX core. This I^2C slave-only controller for SCDC is not required if HDMI 2.0b is not intended.

4.2.1.8. Transceiver Reconfiguration Controller

You can use the Transceiver Reconfiguration Controller IP core to change the device transceiver settings at any time.

You can selectively reconfigure any portion of the transceiver. The reconfiguration of each portion requires a read-modify-write operation (read first, then write). The read-modify-write operation modifies only the appropriate bits in a register and does not affect the other bits.

The Transceiver Reconfiguration Controller is only available and required in Arria V and Stratix V devices. Because the RX and TX transceivers share a single controller, the controller requires Platform Designer interconnects, such as Avalon-MM Master Translator and Avalon-MM Slave Translator, in the Platform Designer system.

- The Avalon-MM Master Translator provides an interface between this controller and the RX Multirate Reconfig Controller.
- The Avalon-MM Slave Translator arbitrates the RX and TX reconfiguration event for this controller.

4.2.1.9. VIP Bypass and Audio, Auxiliary and InfoFrame Buffers

The video data output and synchronization signals from HDMI RX core is looped through a DCFIFO across RX and TX video clock domains. The General Control Packet (GCP), InfoFrames (AVI, VSI, and AI), auxiliary data and audio data are looped through DCFIFOs across RX and TX link speed clock domains.

The auxiliary data port of the HDMI TX core controls the auxiliary data that flow through DCFIFO through backpressure. The backpressure ensures there is no incomplete auxiliary packet on the auxiliary data port. This block also performs external filtering on the audio data and audio clock regeneration packet from the auxiliary data stream before sending to the HDMI TX core auxiliary data port.

4.2.1.10. Transceiver Native PHY (TX)

The Arria V and Stratix V Transceiver Native PHY (TX) configuration settings are typically the same as RX.

Table 12. Arria V and Stratix V Transceiver Native PHY (TX) Configuration Settings (6,000 Mbps)

This table shows an example of Arria V and Stratix V Transceiver Native PHY (TX) configuration settings for TMDS bit rate of 6,000 Mbps.

Parameters	Settings
Datapath Options	
Enable TX datapath	On
Enable RX datapath	Off
Enable Standard PCS	On
Initial PCS datapath selection	Standard
Number of data channels	4
Bonding mode	xN
Enable simplified data interface	On
TX PMA	
Data rate	6,000 Mbps
TX local clock division factor	1
Enable TX PLL dynamic reconfiguration	On
Use external TX PLL	Off
Number of TX PLLs	1
Main TX PLL logical index	0
Number of TX PLL reference clocks	1
PLL type	CMU

continued...

TX PMA	
Reference clock frequency	600 MHz
Selected reference clock source	0
Selected clock network	xN

Standard PCS	
Standard PCS protocol	Basic
Standard PCS/PMA interface width	• 10 (for 1 symbol per clock) • 20 (for 2 and 4 symbols per clock)
Enable TX byte serializer	• Off (for 1 and 2 symbols per clock) • On (for 4 symbols per clock)

Table 13. Arria V and Stratix V Transceiver Native PHY (TX) Common Interface Ports

This table describes the Arria V and Stratix V Transceiver Native PHY (TX) common interface ports.

Signals	Direction	Description
Clocks		
`tx_pll_refclk`	Input	The reference clock input to the TX PLL.
`tx_std_clkout[3:0]`	Output	TX parallel clock output.
`tx_std_coreclkin[3:0]`	Input	TX parallel clock that drives the write side of the TX phase compensation FIFO. Connect to `tx_std_clkout[0]` ports.
Resets		
`tx_analogreset[3:0]`	Input	When asserted, resets all the blocks in TX PMA. Connect to Transceiver PHY Reset Controller (TX) IP core.
`tx_digitalreset[3:0]`	Input	When asserted, resets all the blocks in TX PCS. Connect to the Transceiver PHY Reset Controller (TX) IP core.
TX PLL		
`pll_powerdown`	Input	When asserted, resets the TX PLL. Connect to the Transceiver PHY Reset Controller (TX) IP core.
`pll_locked`	Output	When asserted, indicates that the TX PLL is locked. Connect to the Transceiver PHY Reset Controller (TX) IP core.
PCS Ports		
`unused_tx_parallel_data`	Input	Leave unconnected.
`tx_parallel_data[S*4*10-1:0]`	Input	PCS TX parallel data. *Note:* S=Symbols per clock.
PMA Port		
`tx_serial_data[3:0]`	Output	TX differential serial output data.

Calibration Status Port		
tx_cal_busy[3:0]	Output	When asserted, indicates that the initial TX calibration is in progress. This port is also asserted if the reconfiguration controller is reset. Connect to the Transceiver PHY Reset Controller (TX) IP core.

Reconfiguration Ports		
reconfig_to_xcvr[349:0]	Input	Reconfiguration signals from the Transceiver Reconfiguration Controller.
reconfig_from_xcvr[229:0]	Output	Reconfiguration signals to the Transceiver Reconfiguration Controller.

4.2.1.11. Transceiver PHY Reset Controller

The Transceiver PHY Reset Controller IP core ensures a reliable initialization of the RX and TX transceivers.

The reset controller has separate reset controls per channel to handle synchronization of reset inputs, lagging of PLL locked status, and automatic or manual reset recovery mode.

4.2.1.12. Oversampler (TX)

The Oversampler (TX) transmits data by repeating each bit of the input word a given number of times and constructs the output words.

The oversampling factor is fixed at 5. The Oversampler (TX) assumes that the input word is only valid every 5 clock cycles. This block enables when the outgoing data stream is determined to be below the TX transceiver minimum link rate by reading once from the DCFIFO every 5 clock cycles.

4.2.1.13. Clock Enable Generator

The Clock Enable Generator is a logic that generates a clock enable pulse.

This clock enable pulse asserts every 5 clock cycles and serves as a read request signal to clock the data out from DCFIFO.

4.2.1.14. Platform Designer System

The Platform Designer system consists of the VIP passthrough for HDMI video stream, source SDC controller, and source reconfiguration controller blocks.

4.2.1.14.1. VIP Passthrough for HDMI Video Stream

For certain example designs, you can loop the video data output and synchronization signals from HDMI RX core through the VIP data path.

The Clocked Video Input II (CVI II) Intel FPGA IP core converts clocked video formats to Avalon-ST video by stripping incoming clocked video of horizontal and vertical blanking, leaving only active picture data.

- The IP core provides clock crossing capabilities to allow video formats running at different frequencies to enter the system.
- The IP core also detects the format of the incoming clocked video and provides this information in a set of registers.
- The Nios II processor uses this information to reconfigure the video frame mode registers of the CVO IP core in the VIP passthrough design.

The Video Frame Buffer II Intel FPGA IP core buffers video frames into external RAM.

- The IP core supports double and triple buffering with a range of options for frame dropping and repeating.
- You can use the buffering options to solve throughput issues in the data path and perform simple frame rate conversion.

In a VIP passthrough design, you can reference the HDMI source PLL and sink PLL using separate clock sources. However, in a VIP bypass design, you must reference the HDMI source PLL and sink PLL using the same clock source.

The Clocked Video Output II (CVO II) Intel FPGA IP core converts data from the flow-controlled Avalon-ST video protocol to clocked video.

- The IP core provides clock crossing capabilities to allow video formats running at different frequencies to be created from the system.
- It formats the Avalon-ST video into clocked video by inserting horizontal and vertical blanking and generating horizontal and vertical synchronization information using the Avalon-ST video control and active picture packets.
- The video frame is described using the mode registers that are accessed through the Avalon-MM control port.

Table 14. Difference between VIP Passthrough Design and VIP Bypass Design

VIP Passthrough Design	VIP Bypass Design
• Can reference the HDMI source PLL and sink PLL using separate clock sources • Demonstrates only certain video formats—640×480p60, 720×480p60, 1280×720p60, 1920×1080p60, and 3840×2160p24	• Must reference the HDMI source PLL and sink PLL using the same clock source • Demonstrates all video formats.

Table 15. VIP Passthrough and VIP Bypass Options for the Supported Devices

Device Family	Symbols Per Clock	HDMI Specification Support	Bitec HDMI HSMC 2.0 Daughter Card	Directory	VIP Passthrough	VIP Bypass
Arria V	2	1.4b	HSMC (Rev8)	av_sk	Supported	Supported
	4	2.0b	HSMC (Rev8)	av_sk_hdmi2	Not supported	Supported
Stratix V	2	2.0b	HSMC (Rev8)	sv_hdmi2	Not supported	Supported

4.2.1.14.2. Source SCDC Controller

The source SCDC Controller contains the I^2C master controller. The I^2C master controller transfers the SCDC data structure from the FPGA source to the external sink for HDMI 2.0b operation.

For example, if the outgoing data stream is 6,000 Mbps, the Nios II processor commands the I^2C master controller to update the `TMDS_Bit_Clock_Ratio` and `Scrambler_Enable` bits of the sink TMDS configuration register to 1. The same I^2C master can also transfer the DDC data structure (E-EDID) between the HDMI source and external sink.

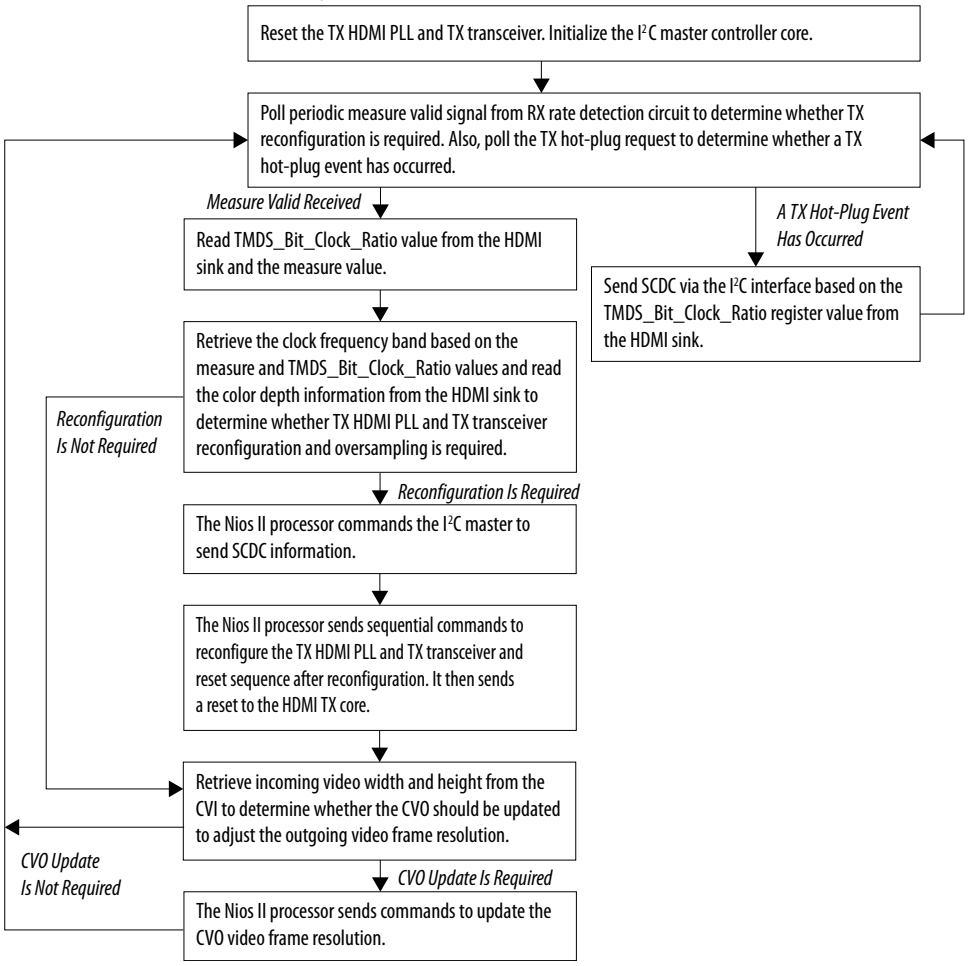
4.2.1.14.3. Source Reconfiguration Controller

The Nios II CPU acts as the multirate reconfiguration controller for the HDMI source.

The CPU relies on the periodic rate detection from the Multirate Reconfig Controller (RX) to determine if TX requires reconfiguration. The Avalon-MM slave translator provides the interface between the Nios II processor Avalon-MM master interface and the Avalon-MM slave interfaces of the externally instantiated HDMI source's PLL Reconfig Intel FPGA IP and Transceiver Native PHY (TX).

Figure 10. Nios II Software Flow

The reconfiguration sequence flow for TX is the same as RX, except that the PLL and transceiver reconfiguration, and the reset sequence is performed sequentially. The figure illustrates the Nios II software flow that involves the controls for CVO, I²C master and HDMI source.



4.2.2. HDMI Hardware Design Requirements

The HDMI design requires an Intel FPGA board and supporting hardware.

- Intel FPGA board
- Bitec HDMI HSMC 2.0 daughter card
- Standard HDMI source—for example, PC with a graphic card and HDMI output
- Standard HDMI sink—for example, monitor with HDMI input
- 2 HDMI cables
  - A cable to connect the graphics card to the Bitec daughter card RX connector.
  - A cable to connect the Bitec daughter card TX connector to the monitor.

Table 16. Intel FPGA Boards and Bitec HDMI HSMC 2.0 Daughter Cards Supported for the Design

Design Example	Intel FPGA Board	Bitec HDMI HSMC 2.0 Daughter Card
Arria V (av_sk)	Arria V GX FPGA Starter Kit	HSMC (Rev8)
Arria V (av_sk_hdmi2)	Arria V GX FPGA Starter Kit	HSMC (Rev8)
Stratix V (sv_hdmi2)	Stratix V GX FPGA Development Kit	HSMC (Rev8)

Related Information

- Arria V GX Starter Kit User Guide
- Stratix V GX FPGA Development Kit User Guide

4.2.3. Design Walkthrough

Setting up and running the HDMI hardware design consists of four stages.

You can use the Intel-provided scripts to automate these stages.

1. Set up the hardware.
2. Copy the design files to your working directory.
3. Build and compile the design.
4. View the results.

4.2.3.1. Set Up the Hardware

The first stage of the demonstration is to set up the hardware.

To set up the hardware for the demonstration:

1. Connect the Bitec HDMI HSMC 2.0 daughter card to the FPGA development board.
2. Connect the FPGA board to your PC using a USB cable.

   Note: The Arria V GX FPGA Starter Kit and Stratix V GX FPGA Development Kit have an On-Board Intel FPGA Download Cable II connector. If your version of the board does not have this connector, you can use an external Intel FPGA Download Cable cable.
3. Connect an HDMI cable from the HDMI RX connector on the Bitec HDMI HSMC 2.0 daughter card to a standard HDMI source, in this case a PC with a graphic card and HDMI output.
4. Connect another HDMI cable from the HDMI TX connector on the Bitec HDMI HSMC 2.0 daughter card to a standard HDMI sink, in this case a monitor with HDMI input.

4.2.3.2. Copy the Design Files

After you set up the hardware, you copy the design files. Copy the hardware demonstration files from one of the following paths to your working directory:

- Arria V
  - 2 symbols per clock (HDMI 1.4b) demonstration: `<IP root directory>/altera_hdmi/hw_demo/av_sk`
  - 4 symbols per clock (HDMI 2.0b) demonstration: `<IP root directory>/altera_hdmi/hw_demo/av_sk_hdmi2`
- Stratix V
  - 2 symbols per clock (HDMI 2.0b) demonstration: `<IP root directory>/altera_hdmi/hw_demo/sv_hdmi2`

4.2.3.3. Build and Compile the Design

After you copy the design files, you can build the design.

You can use the provided Tcl script to build and compile the FPGA design.

1. Open a Nios II Command Shell.
2. Change the directory to your working directory.
3. Type the command and enter `source runall.tcl`.
   This script executes the following commands:
   - Generate IP catalog files
   - Generate the Platform Designer system
   - Create a Intel Quartus Prime project
   - Create a software work space and build the software
   - Compile the Intel Quartus Prime project
   - Run Analysis & Synthesis to generate a post-map netlist for DDR assignments —for VIP passthrough design only
   - Perform a full compilation

   Note: If you are a Linux user, you will get a message `cygpath: command not found`. You can safely ignore this message; the script will proceed to generate the next commands.

4.2.3.4. View the Results

At the end of the demonstration, you will be able to view the results on the on the standard HDMI sink (monitor).

To view the results of the demonstration, follow these steps:

1. Power up the Intel FPGA board.
2. Type the following command on the Nios II Command Shell to download the Software Object File (`.sof`) to the FPGA.

   `nios2-configure-sof output_files/`<Quartus project name>.sof
3. Power up the standard HDMI source and sink (if you haven't done so).
   The design displays the output of your video source (PC).

Note: If the output does not appear, press `cpu_resetn` to reinitialize the system or perform HPD by unplugging the cable from the standard source and plug it back again.

4. Open the graphic card control utility (if you are using a PC as source). Using the control panel, you can switch between various video resolutions.

   The av_hdmi2 and sv_hdmi2 demonstration designs allow any video resolutions up to 4Kp60. The av_sk design allows *640×480p60*, *720×480p60*, *1280×720p60*, *1920×1080p60*, and *3840×2160p24* when you select the VIP passthrough mode (`user_dipsw[0] = 0`). If you select the VIP bypass mode (`user_dipsw[0] = 1`, the design allows any video resolutions up to 4Kp60.

4.2.3.4.1. Push Buttons, DIP Switches and LED Functions

Use the push buttons, DIP switches, and LED functions on the board to control your demonstration.

Table 17. Push Buttons, DIP Switches and LEDs Functions

Push Button/ DIP Switch/LED	Pins		Functions
	av_sk/av_sk_hdmi2	sv_hdmi2	
cpu_resetn	D5	AM34	Press once to perform system reset.
user_pb[0]	A14	A7	Press once to turn on and turn off HPD signal to the standard HDMI source.
user_pb[1]	B15	B7	Press and hold to instruct the TX to send DVI encoded signal and release to send HDMI encoded signal.
user_pb[2]	B14	C7	Press and hold to instruct the TX to stop sending InfoFrames and release to resume sending.
user_dipsw[0]	D15	Unused	Only used in av_sk design which demonstrates the VIP passthrough feature. • 0: VIP passthrough • 1: VIP bypass
user_led[0]	F17	J11	RX HDMI PLL lock status. • 0: Unlocked • 1: Locked
user_led[1]	G15	U10	RX transceiver ready status. • 0: Not ready • 1: Ready
user_led[2]	G16	U9	RX HDMI core lock status • 0: At least 1 channel unlocked • 1: All 3 channels locked
user_led[3]	G17	AU24	RX oversampling status. • 0: Non-oversampled (more than 611 Mbps for av_sk and sv_hdmi2, more than 1,000 Mbps for av_sk_hdmi2) • 1: Oversampled (less than 611 Mbps for av_sk and sv_hdmi2, less than 1,000 Mbps for av_sk_hdmi2)
user_led[4]	D16	AF28	TX HDMI PLL lock status.

continued...

Push Button/ DIP Switch/LED	Pins		Functions
	av_sk/av_sk_hdmi2	sv_hdmi2	
			• 0: Unlocked • 1: Locked
user_led[5]	C13	AE29	TX transceiver ready status. • 0: Not ready • 1: Ready
user_led[6]	C14	AR7	TX transceiver PLL lock status. • 0: Unlocked • 1: Locked
user_led[7]	C16	AV10	TX oversampling status. • 0: Non-oversampled (more than 611 Mbps for av_sk and sv_hdmi2, more than 1,000 Mbps for av_sk_hdmi2) • 1: Oversampled (less than 611 Mbps for av_sk and sv_hdmi2, less than 1,000 Mbps for av_sk_hdmi2)

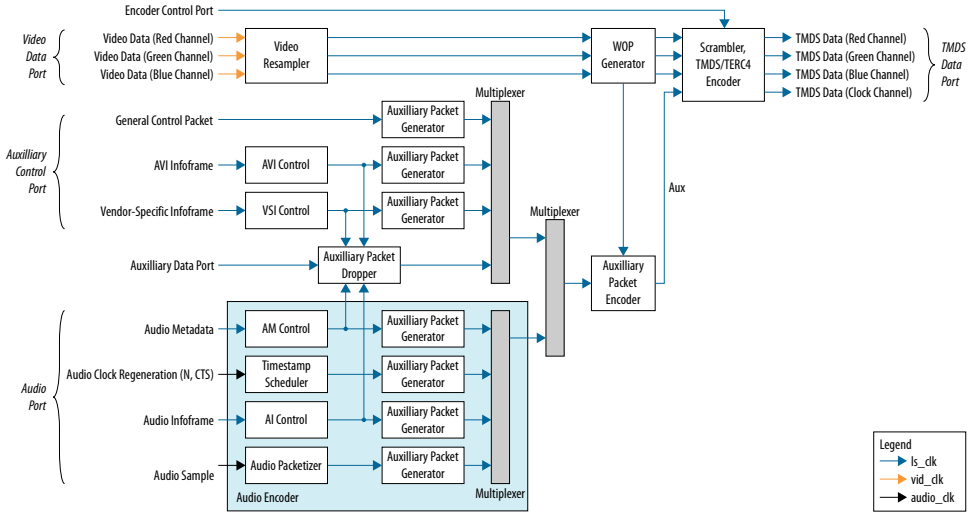
5. HDMI Source

5.1. Source Functional Description

The HDMI source core provides direct connection to the Transceiver Native PHY through a 10-bit, 20-bit, or 40-bit parallel data path.

Figure 11. HDMI Source Signal Flow Diagram

The figure below shows the flow of the HDMI source signals. The figure shows the various clocking domains used within the core.



The source core provides four 10-bit, 20-bit or 40-bit parallel data paths corresponding to the 3 color channels and the clock channel.

The source core accepts video, audio, and auxiliary channel data streams. The core produces a scrambled and TMDS/TERC4 encoded data stream that would typically connect to the high-speed transceiver parallel data inputs.

Note: The scrambled data only applies for HDMI 2.0b stream with TMDS Bit Rate higher than 3.4 Gbps.

Central to the core is the Scrambler, TMDS/TERC4 Encoder. The encoder processes either video or auxiliary data.

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

5.1.1. Source Scrambler, TMDS/TERC4 Encoder

The TMDS/TERC4 encoder implements 8-bit to 10-bit and 4-bit to 10-bit algorithms as defined in the *HDMI 1.4b Specification Section 5.4*. Each data channel, with exception of the clock channel, has its own encoder. You can configure the core to enable scrambling, as defined in the *HDMI 1.4b Specification Section 6.1.2*, before TMDS/TERC4 encoding.

The encoder processes symbol data at 1, 2, or 4 symbols per clock. When the encoder operates in 2 or 4 symbols per clock, it also produces the output in the form of two or four encoded symbols per clock.

The TMDS/TERC4 encoder also produces digital visual interface (DVI) signaling when you deassert the `mode` input signal. DVI signaling is identical to HDMI signaling, except for the absence of data and video islands and TERC4 auxiliary data.

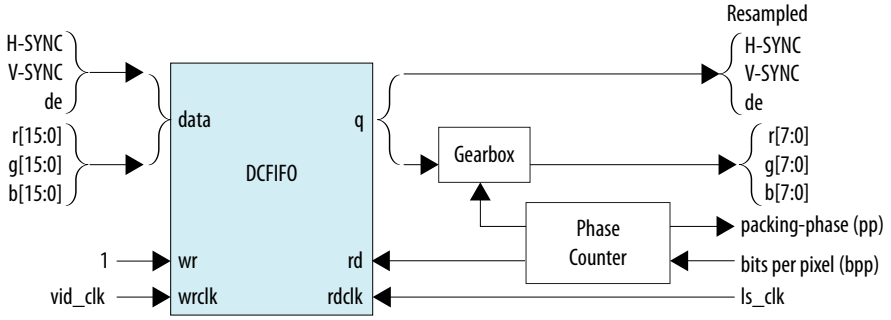
5.1.2. Source Video Resampler

The video resampler consists of a dual-clock FIFO (DCFIFO) and a gearbox.

The gearbox converts data of 8, 10, 12, or 16 bits per component to 8-bit per component data based on the current color depth. The General Control Packet (GCP) conveys the color depth information.

Figure 12. Source Video Resampler Signal Flow Diagram

The figure below shows the components of the video resampler and the signal flow between these components.



The resampler adheres to the recommended phase encoding method described in *HDMI 1.4b Specification Section 6.5*.

- The phase counter must register the last pixel packing-phase (pp) of the last pixel of the last active line.
- The core then transmits the pp value to the attached sink device in the GCP for packing synchronization.

The HDMI cable may send across four different pixel encodings: RGB 4:4:4, YCbCr 4:4:4, and YCbCr 4:2:2 (as described in *HDMI 1.4b Specification Section 6.5*), and YCbCr 4:2:0 (as described in *HDMI 2.0b Specification Section 7.1*).

Figure 13. Pixel Data Input Format RGB/YCbCr 4:4:4

The figure below shows the RGB/YCbCr 4:4:4 color space pixel bit-field mappings per symbol. When the actual color depth is below 16 bpc, the unused LSBs are set to zero.

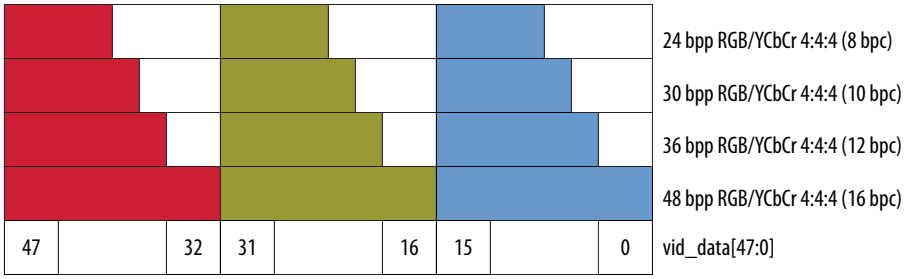
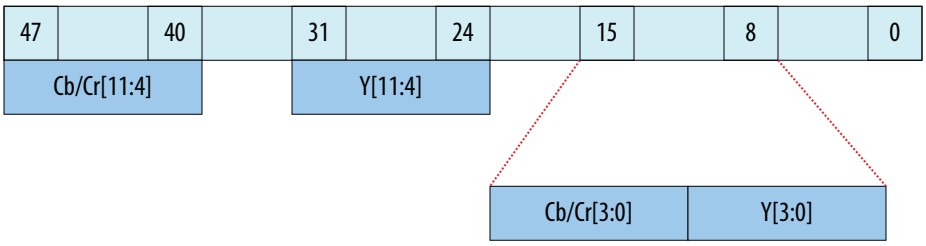


Figure 14. Pixel Data Input Format YCbCr 4:2:2 (12 bpc)

The figure below shows the YCbCr 4:2:2 color space pixel bit-field mappings per symbol. As with 4:4:4 color space, the unused LSBs are set to zero.

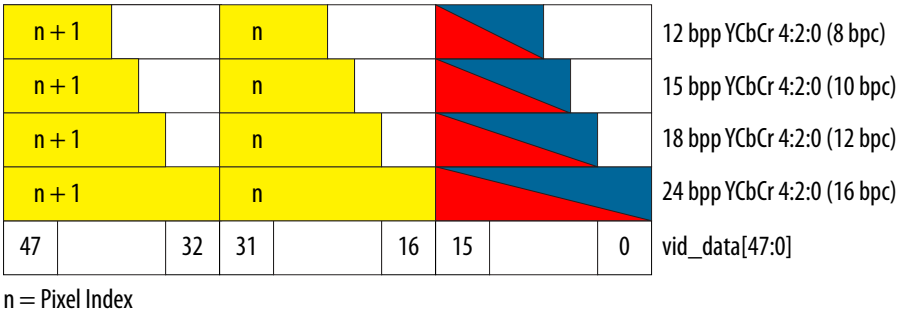


The higher order 8 bits of the Y samples are mapped to the 8 bits of Channel 1 and the lower order 4 bits are mapped to the lower order 4 bits of Channel 0.

The first pixel transmitted within a Video Data Period contains three components, Y0, Cb0 and Cr0. The Y0 and Cb0 components are transmitted during the first pixel period while Cr0 is transmitted during the second pixel period. This second pixel period also contains the only component for the second pixel, Y1. In this way, the link carries one Cb sample for every two pixels and one Cr sample for every two pixels. These two components (Cb and Cr) are multiplexed onto the same signal paths on the link.

Figure 15. Pixel Data Input Format YCbCr 4:2:0

The figure shows the YCbCr 4:2:0 color space pixel bit-field mappings. As with 4:4:4 color space, the unused LSBs are set to zero.



The two horizontally successive 8-bit Y components are transmitted in TMDS Channels 1 and 2, in that order. The 8-bit Cb or Cr components are transmitted alternately in TMDS Channel 0, line by line.

For even lines starting with line 0:

- `vid_data[47:32]` always transfer the Yn+1 component
- `vid_data[31:16]` always transfer the Yn component
- `vid_data[15:0]` always transfer the Cbn component

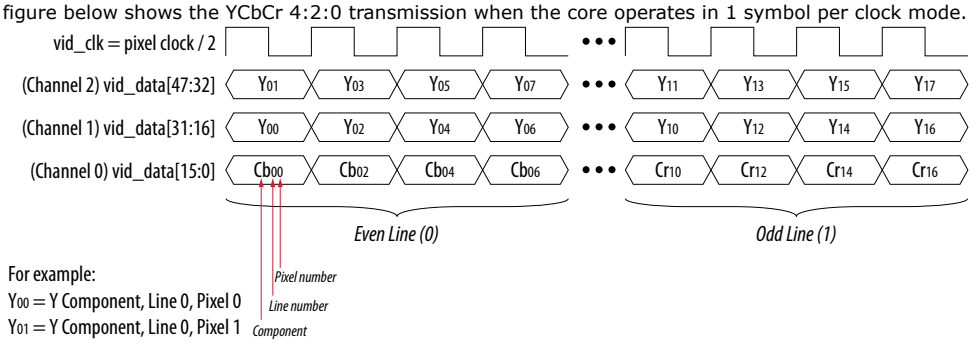
For odd lines:

- `vid_data[47:32]` always transfer the Yn+1 component
- `vid_data[31:16]` always transfer the Yn component
- `vid_data[15:0]` always transfer the Crn component

The frequency of `vid_clk` must be halved when YCbCr 4:2:0 is used, because two pixels are fed into a single clock cycle.

Figure 16. YCbCr 4:2:0 Transport Using 1 Symbol Per Clock Mode

The figure below shows the YCbCr 4:2:0 transmission when the core operates in 1 symbol per clock mode.



5.1.3. Source Window of Opportunity Generator

The source Window of Opportunity (WOP) generator creates valid data islands within the blanking regions.

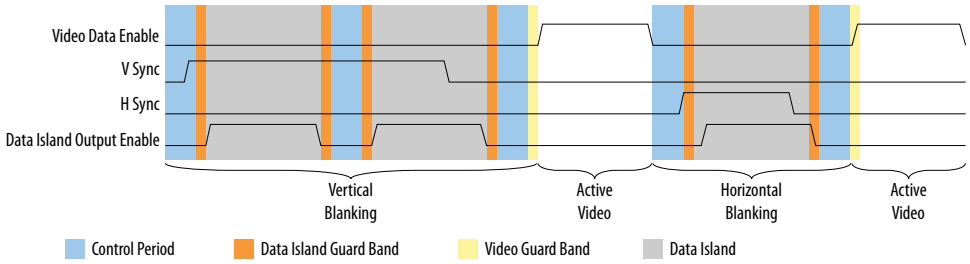
During horizontal blanking region, the WOP generator creates a leading region to hold at least 12 period symbols that include eight preamble symbols. The generator also creates a trailing region to hold two data island trailing guard band symbols, at least 12 control period symbols that include eight preamble symbols and two video leading guard band symbols.

During vertical blanking region, the source cannot send more than 18 auxiliary packets consecutively. The WOP generator deasserts the data island output enable (`aux_wop`) line after every 18th auxiliary packet for 32-symbol clocks.

The WOP generator also has an integral number of auxiliary packet cycles: 24 clocks when processing in 1-symbol mode, 16 clocks when processing in 2-symbol mode, and 8 clocks when processing in 4-symbol mode.

Figure 17. Typical Window of Opportunity

The figure below shows a typical output from the WOP generator.



5.1.4. Source Auxiliary Packet Encoder

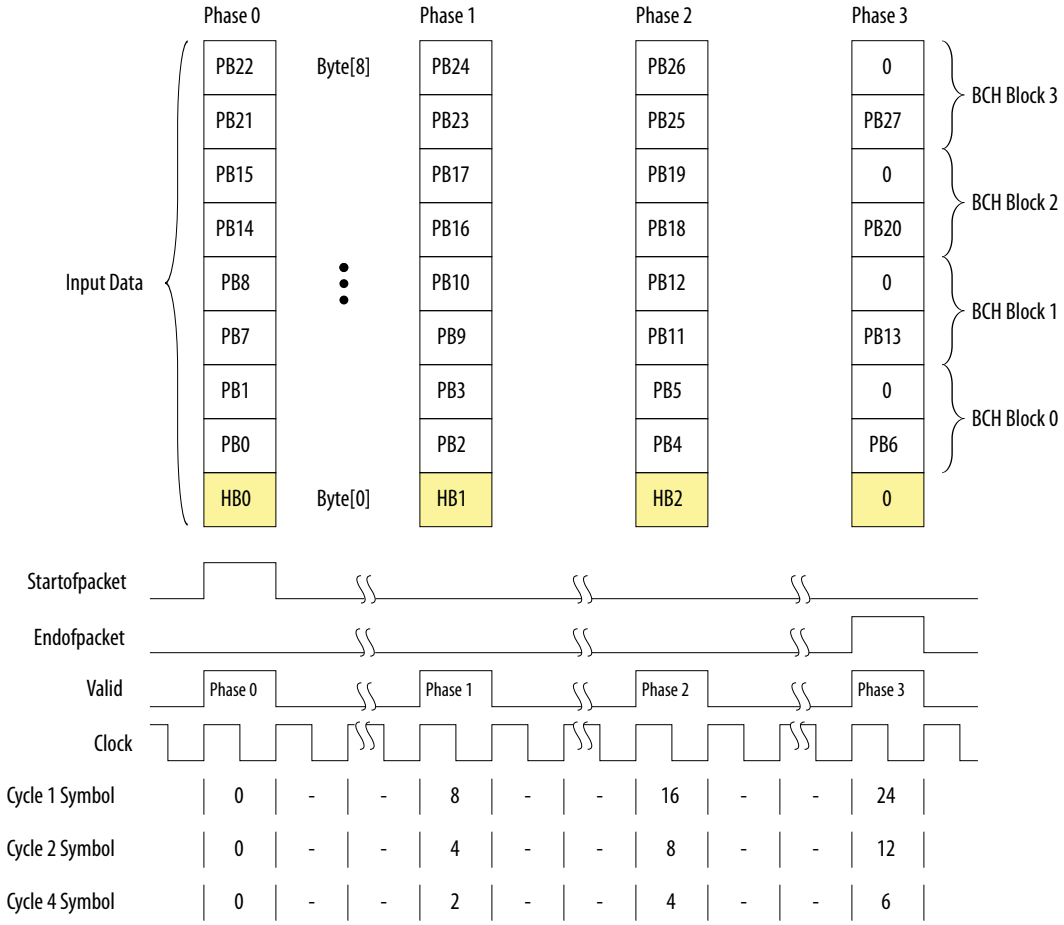
Auxiliary packets are encoded by the source auxiliary packet encoder.

The auxiliary packets originate from several sources, which are multiplexed into the auxiliary packet encoder in a round-robin schedule. The auxiliary packet encoder converts a standard stream into the channel data format required by the TERC4 encoder.

The auxiliary packet encoder also calculates and inserts the Bose-Chaudhuri-Hocquenghem (BCH) error correction code.

Figure 18. Auxiliary Packet Encoder Input

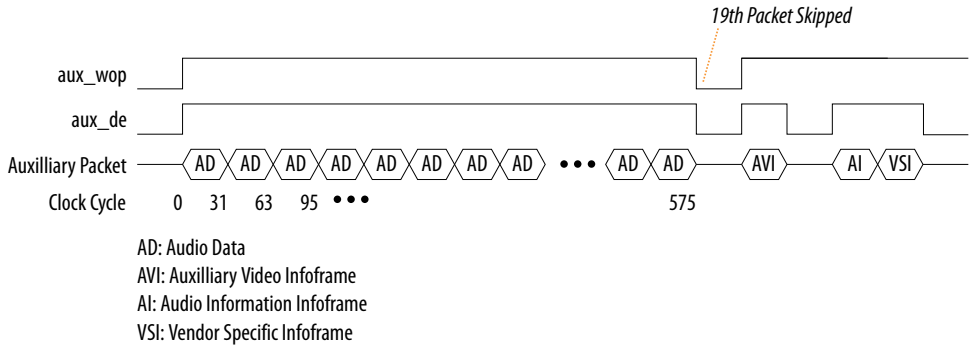
The figure below shows the auxiliary packet encoder input from a 72-bit input data.



The encoder assumes the data valid input will remain asserted for the duration of a packet to complete. A packet is always 24 clocks (in 1-symbol mode), 12 clocks (in 2-symbol mode), or 6 clocks (in 4-symbol mode).

Figure 19. Typical Auxiliary Packet Stream During Blanking Interval

The figure below shows a typical auxiliary packet stream in 1-symbol per clock mode, where 0 denotes a null packet.



5.1.5. Source Auxiliary Packet Generators

The source core uses various auxiliary packet generators. The packet generators convert the packet field inputs to the auxiliary packet stream format.

The packet generator propagates backpressure from the output ready signal to the input ready signal. The generator asserts the input valid signal when a packet is ready to be transmitted. The input valid signal remains asserted until the end of the packet and the generator receives a ready acknowledgment.

5.1.6. Source Auxiliary Data Path Multiplexers

The auxiliary data path multiplexers provide paths for the various auxiliary packet generators.

The various auxiliary packet generators traverse a multiplexed routing path to the auxiliary packet encoder. The multiplexers obey a round-robin schedule and propagate backpressure.

5.1.7. Source Auxiliary Control Port

To simplify the user logic, the source core has control ports to send the most common auxiliary control packets.

These packets are: General Control Packet, Auxiliary Video Information (AVI) InfoFrame, and HDMI Vendor Specific InfoFrame (VSI).

The core sends the default values in the auxiliary packets. The default values allow the core to send video data compatible with the *HDMI 1.4b Specification* with minimum description.

You can also override the generators using the customized input values. The override values replace the default values when the input checksum is non-zero.

Table 18. Insertion and Filtration

Auxiliary Packets		Insertion/Filtration	Frequency of Insertion
General Control Packet (GCP)	–	The core always inserts GCP packets from the GCP sideband upon the rising edge of `vsync`. The core always removes the GCP in the Auxiliary Data Port. You must provide the pixel packing and color depth information through the `gcp` port.	Once per frame.
Auxiliary Video Information (AVI) InfoFrame	info_avi[112]=1'b0	The core inserts `info_avi[111:0]` when there is a non-zero bit upon the rising edge of `vsync`. The core send default values when all bits are zero. The core filters the AVI infoframe packet on the Auxiliary Data Port.	Once per frame.
	info_avi[112]=1'b1	The core does not insert `info_avi[111:0]`. The AVI InfoFrame packet on the Auxiliary Data Port passes through.	

continued...

Auxiliary Packets		Insertion/Filtration	Frequency of Insertion
Vendor Specific InfoFrame (VSI)	info_vsi[61]=1'b0	The core inserts `info_vsi[60:0]` when there is a non-zero bit upon the rising edge of `vsync`. The core sends default values when all bits are zero. The core filters the VSI InfoFrame packet on the Auxiliary Data Port.	Once per frame.
	info_vsi[61]=1'b1	The core does not insert `info_vsi[60:0]`. The VSI InfoFrame packet on the Auxiliary Data Port passes through.	
Audio Metadata (AM)	audio_metadata[165]=1'b0	The core inserts audio_metadata[164:0] when `audio_format[3:0]` is 3D audio or MST audio upon the rising edge of `vsync`. The core filters the AM packet on the Auxiliary Data Port.	Once per frame.
	audio_metadata[165]=1'b1	The core does not insert `audio_metadata[164:0]`. The AM packet on the Auxiliary Data Port passes through.	
Audio InfoFrame (AI)	audio_info_ai[48]=1'b0	The core inserts `audio_info_ai[47:0]` when there is a non-zero bit upon the rising edge of `vsync`. The core sends default values when all bits are zero. The core filters the AI packet on the Auxiliary Data Port.	Once per frame.
	audio_info_ai[48]=1'b1	The core does not insert `audio_info_ai[47:0]`. The AI packet on the Auxiliary Data Port passes through.	
Audio Control Regeneration (ACR)	–	The core always inserts the `audio_N` and `audio_CTS`. The core does not filter the ACR packet in the auxiliary. If there is ACR packet in the Auxiliary Data Port, you must remove it before passing into the Auxiliary Data Port.	Every 1 ms.
Audio Sample	–	The core always inserts `audio_data`. The core does not filter the audio sample packet in the Auxiliary Data Port. If there is audio sample packet in the Auxiliary Data Port, you must remove it before passing into the Auxiliary Data Port.	Based on audio sample rate.

5.1.7.1. Source General Control Packet (GCP)

Table 19. Source GCP Bit-Fields

This table lists the controllable bit-fields for the Source `gcp[5:0]` port.

Bit Field	Name	Value				Comment
gcp[3:0]	Color Depth (CD)	CD3	CD2	CD1	CD0	Color depth
		0	0	0	0	Color depth not indicated
		0	1	0	0	8 bpc or 24 bits per pixel (bpp)

continued...

Bit Field	Name	Value				Comment
		0	1	0	1	10 bpc or 30 bpp
		0	1	1	0	12 bpc or 36 bpp
		0	1	1	1	16 bpc or 48 bpp
		Others				Reserved
gcp[4]	Set_AVMUTE	Refer to *HDMI 1.4b Specification Section 5.3.6*.				
gcp[5]	Clear_AVMUTE	Refer to *HDMI 1.4b Specification Section 5.3.6*.				

All other fields for the source GCP, (for example, Pixel Packing Phase and Default Phase as described in *HDMI 1.4b Specification Section 5.3.6*) are calculated automatically inside the core. You must provide the bit-field values in the table above through the source `gcp[5:0]` port. The GCP on the Auxiliary Data Port will always be filtered.

5.1.7.2. Source Auxiliary Video Information (AVI) InfoFrame Bit-Fields

Table 20. Source Auxiliary Video Information (AVI) InfoFrame

The table below lists the bit-fields for the AVI InfoFrame port bundle (as described in *HDMI 1.4b Specification Section 8.2.1*).

The signal bundle is clocked by `ls_clk`.

Bit-field	Name	Description	Default Value
7:0	Checksum	Checksum	8'h67
9:8	S	Scan information	2'h0
11:10	B	Bar info data valid	2'h0
12	A0	Active information present	1'h0
14:13	Y	RGB or YCbCr indicator	2'h0
15	Reserved	Returns 0	1'h0
19:16	R	Active format aspect ratio	4'h8
21:20	M	Picture aspect ratio	2'h0
23:22	C	Colorimetry (for example: ITU BT.601, BT.709)	2'h0
25:24	SC	Non-uniform picture scaling	2'h0
27:26	Q	Quantization range	2'h0
30:28	EC	Extended colorimetry	3'h0
31	ITC	IT content	1'h0
38:32	VIC	Video format identification code	7'h00
39	Reserved	Returns 0	1'h0
43:40	PR	Picture repetition factor	4'h0
45:44	CN	Content type	2'h0
47:46	YQ	YCC quantization range	2'h0

continued...

Bit-field	Name	Description	Default Value
63:48	ETB	Line number of end of top bar	16'h0000
79:64	SBB	Line number of start of bottom bar	16'h0000
95:80	ELB	Pixel number of end of left bar	16'h0000
111:96	SRB	Pixel number of start of right bar	16'h0000
112	Control	Disables the core from inserting the InfoFrame packet. • 1: The core does not insert `info_avi[111:0]`. The AVI InfoFrame packet on the Auxiliary Data Port passes through. • 0: The core inserts `info_avi[111:0]` when there is a non-zero bit. The core sends default values when all bits are zero. The core filters the AVI InfoFrame packet on the Auxiliary Data Port.	–

5.1.7.3. Source HDMI Vendor Specific InfoFrame (VSI)

Table 21. Source HDMI Vendor Specific InfoFrame Bit-Fields

The table below lists the bit-fields for VSI (as described in *HDMI 1.4b Specification Section 8.2.3*).

The signal bundle is clocked by `ls_clk`.

Bit-field	Name	Description	Default Value
4:0	Length	Length of HDMI VSI payload	5'h06
12:5	Checksum	Checksum	8'h69
36:13	IEEE	24-bit IEEE registration identifier (0×000C03)	24'h000C03
41:37	Reserved	Reserved (0)	5'h00
44:42	HDMI_Video_Format	Structure of extended video formats exclusively defined in *HDMI 1.4b Specification*	3'h0
52:45	HDMI_VIC or 3D_Structure	• If HDMI_Video_Format = 3'h1, [52:45] = HDMI proprietary video format identification code • If HDMI_Video_Format = 3'h2, [52:49] = 3D_Structure and [48:45] = Reserved (0)	8'h00
57:53	Reserved	Reserved (0)	5'h00
60:58	3D_Ext_Data	3D extended data	3'h0
61	Control	Disables the core from inserting the InfoFrame packet. • 1: The core does not insert `info_vsi[60:0]`. The VSI InfoFrame packet on the Auxiliary Data Port passes through. • 0: The core inserts `info_vsi[60:0]` when there is a non-zero bit. The core sends default values when all bits are zero. The core filters the VSI InfoFrame packet on the Auxiliary Data Port.	–

5.1.8. Source Audio Encoder

Audio transport allows four packet types:

- Audio Clock Regeneration
- Audio InfoFrame
- Audio Metadata
- Audio Sample

The Audio Clock Regeneration packet contains the CTS and N values. You need to provide these values as recommended in *HDMI 1.4b Specification Section 7.2.1 through 7.2.3* and *HDMI 2.0b Specification Section 9.2.1*. The core schedules this packet to be sent every ms. The timestamp scheduler uses the `audio_clk` and *N* value to determine a 1-ms interval.

The audio data queues on a DCFIFO. The core also uses the DCFIFO to synchronize its clock to `ls_clk`. The Audio Packetizer packs the audio data into the Audio Sample packets according to the specified audio format (as described in *HDMI 1.4b Specification Section 5.3.4*). An Audio Sample packet can contain up to 4 audio samples, based on the required audio sample clock. The core sends the Audio Sample packets whenever there is an available slot in the auxiliary packet stream.

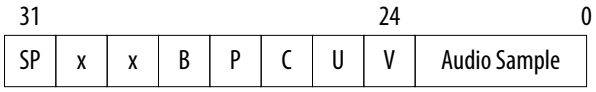
The core determines the payload data packet type from the `audio_format[3:0]` signal.

Table 22. Definition of the Supported audio_format[3:0]

Value	Name	Description
0	Linear Pulse-Code Modulation (LPCM)	Use packet type 0x02 to transport payload data
4	3D Audio (LPCM)	Use packet type 0x0B to transport payload data
6	Multi-Stream(MST) Audio for LPCM	Use packet type 0x0E to transport payload data
Others	–	Reserved

The 32-bit audio data is packed in IEC-60958 standard. The least significant word is the left channel sample.

Figure 20. Audio Data Packing



The fields are defined as:

SP : Sample Present
x : Not Used
B : Start of 192-bit IEC-60958 Channel Status
P : Parity Bit
C : Channel Status
U : User Data Bit
V : Valid Bit

The `audio_data` port is always at a fixed value of 256 bits. In the LPCM format, the core can send up to 8 channels of audio data.

- Channel 1 audio data should be present at `audio_data[31:0]`.
- Channel 2 audio data should be present at `audio_data[63:32]` and so on.

The Sample Present (SP) bit determines whether to use 2-channel or 8-channel layout. If the SP bit from Channel 3 is high, then the core uses the 8-channel layout. If otherwise, the core uses the 2-channel layout. The core ignores all other fields if the SP bit is 0.

The core requires an `audio_de` port for designs in which the `audio_clk` port frequency is higher than the actual audio sample clock. The `audio_de` port qualifies the audio data. If `audio_clk` is the actual audio sample clock, you can tie the `audio_de` signal to 1. For audio channels fewer than 8, insert 0 to the respective audio data of the unused audio channels.

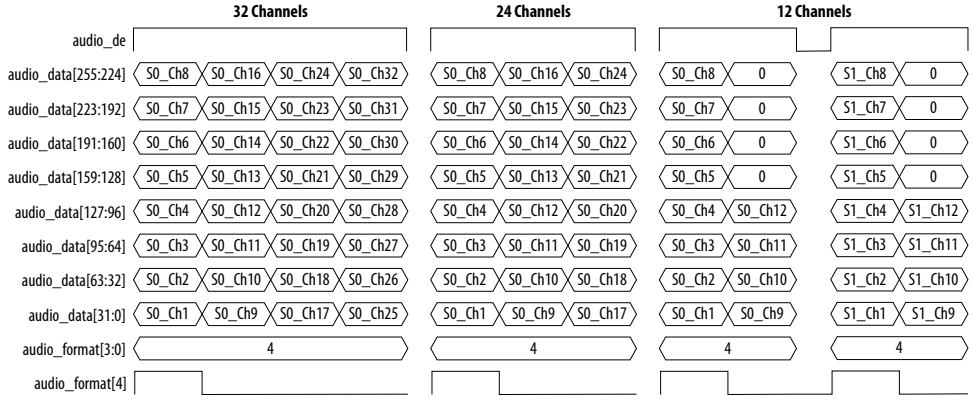
The Audio Clock Regeneration and Audio Sample packets on the Auxiliary Data Port are not filtered by the core. You must filter these packets externally if you want to loop back the auxiliary data stream from the sink.

3D Audio Format

In 3D format, the core sends up to 32 channels audio data by consuming up to 4 writes of 8 channels. Assert `audio_format[4]` to indicate the first 8 channels of each sample. For audio channels greater than 8, do not drive `audio_clk` at actual audio sample clock; instead drive `audio_clk` with `ls_clk` and qualify `audio_data` with `audio_de`.

Figure 21. 3D Audio Input Example

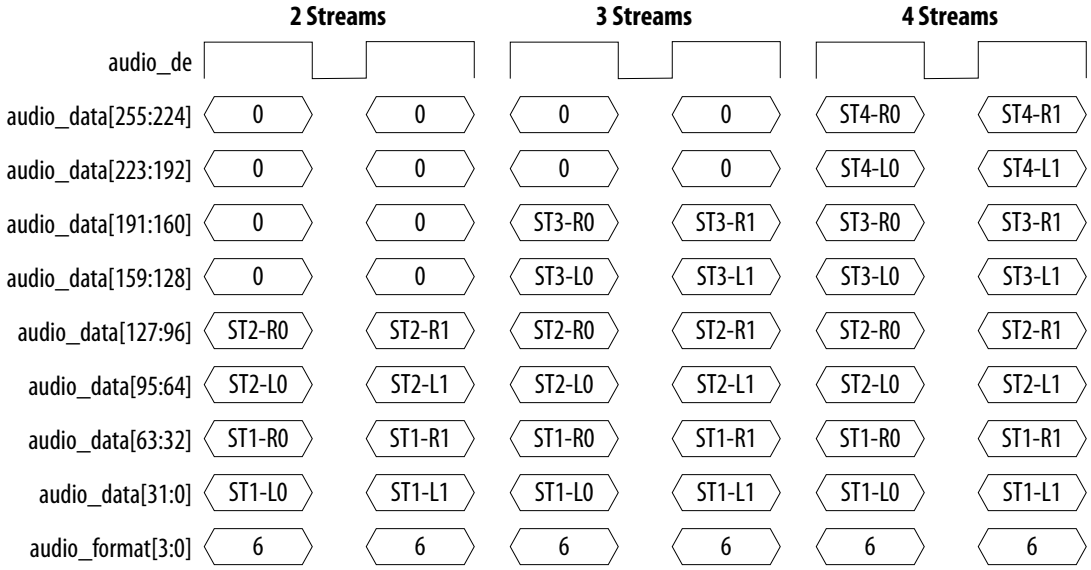
Figure below shows the three examples of 3D audio: Full 32 channels, 24 channels, and 12 channels. In the 12 channels example, the 4 most significant audio channels of the last beat are zero.



MST Audio Format

In MST format, the core sends 2, 3, or 4 streams of audio. For audio streams fewer than 4, you must set the respective audio data to zero for the unused streams as shown in the figure below.

Figure 22. MST Audio Input Example



5.1.8.1. Audio InfoFrame (AI) Bundle Bit-Fields

The core sends the AI default values in the auxiliary packets.

The default values are overridden by the customized input values (`audio_info_ai[47:0]`) when the input checksum is non-zero. The core sends the AI packet on the active edge of the V-SYNC signal to ensure that the packet is sent once per field.

Table 23. Source Audio InfoFrame Bundle Bit-Fields

Table below lists the AI signal bit-fields (as described in *HDMI 1.4b Specification Section 8.2.2*). The signal bundle is clocked by `ls_clk`.

Bit-field	Name	Description	Default Value
7:0	Checksum	Checksum	8'h71
10:8	CC	Channel count	3'h0
11	Reserved	Returns 0	1'h0
15:12	CT	Audio format type	4'h0
17:16	SS	Bits per audio sample	2'h0
20:18	SF	Sampling frequency	3'h0
23:21	Reserved	Returns 0	3'h0
31:24	CXT	Audio format type of the audio stream	8'h00
39:32	CA	Speaker location allocation FL, FR	8'h00
41:40	LFEPBL	LFE playback level information, dB	2'h0
42	Reserved	Returns 0	1'h0

continued...

Bit-field	Name	Description	Default Value
46:43	LSV	Level shift information, dB	4'h0
47	DM_INH	Down-mix inhibit flag	1'h0
48	Control	Disables the core from inserting the AI packet. • 1: The core does not insert `audio_info_ai[47:0]`. The AI packet on the Auxiliary Data Port passes through. • 0: The core inserts `audio_info_ai[47:0]` when there is a non-zero bit. The core sends default values when all bits are zero. The core filters the AI packet on the Auxiliary Data Port.	–

5.1.8.2. Audio Metadata Bundle Bit-Fields

The Audio Metadata (AM) packet carries additional information related to 3D Audio and Multi-Stream Audio (MST).

The core sends the AM packet on the active edge of the `V-SYNC` signal to ensure that the packet is sent once per field. The signal bundle of `audio_metadata[165:0]` is clocked by `ls_clk`.

Table 24. Audio Metadata Bundle Bit-Fields for Packet Header and Control

Table below lists the AM signal bit-fields for packet header (as described in the *HDMI 2.0b Specification Section 8.3*) and control.

Bit-field	Name	Description
0	3D_AUDIO	• 1: Transmits 3D audio • 0: Transmits MST audio
2:1	NUM_VIEWS	Number of views for an MST stream
4:3	NUM_AUDIO_STR	Number of audio streams - 1
165	Control	Disables the core from inserting the AM packet. • 1: The core does not insert `audio_metadata[164:0]`. The AM packet on the Auxiliary Data Port passes through. • 0: The core inserts `audio_metadata[164:0]` when `audio format[3:0]` is 3D audio or MST audio. The core filters the AM packet on the Auxiliary Data Port.

Table 25. Audio Metadata Bundle Bit-Fields for Packet Content when 3D_AUDIO = 1

Table below lists the AM signal bit-fields for packet content when 3D_AUDIO = 1 (as described in the *HDMI 2.0b Specification Section 8.3.1*).

Bit-field	Name	Description
9:5	3D_CC	Channel count of the transmitted 3D audio
12:10	Reserved	Reserved (0)

continued...

Bit-field	Name	Description
16:13	ACAT	Audio channel allocation standard
20:17	Reserved	Reserved (0)
28:21	3D_ACAT	Channel/Speaker allocation for 3D audio
164:29	Reserved	Reserved (0)

Table 26. Audio Metadata Bundle Bit-Fields for Packet Content when 3D_AUDIO = 0

Table below lists the AM signal bit-fields for packet content when 3D_AUDIO = 0 (as described in the *HDMI 2.0b Specification Section 8.3.2*).

Bit-field	Name	Description
5	Multiview_Left_0	Left stereoscopic picture (Subpacket 0 in MST Audio Sample Packet)
6	Multiview_Right_0	Right stereoscopic picture (Subpacket 0 in MST Audio Sample Packet)
12:7	Reserved	Reserved (0)
15:13	Suppl_A_Type_0	Supplementary audio type (Subpacket 0 in MST Audio Sample Packet)
16	Suppl_A_Mixed_0	Mix of main audio components and a supplementary audio track (Subpacket 0 in MST Audio Sample Packet)
17	Suppl_A_Valid_0	Audio stream contains a supplementary audio track (Subpacket 0 in MST Audio Sample Packet)
19:18	Reserved	Reserved (0)
20	LC_Valid_0	Validity of Language_Code (Subpacket 0 in MST Audio Sample Packet)
44:21	Language_Code_0	Audio stream language (Subpacket 0 in MST Audio Sample Packet)
45	Multiview_Left_1	Left stereoscopic picture (Subpacket 1 in MST Audio Sample Packet)
46	Multiview_Right_1	Right stereoscopic picture (Subpacket 1 in MST Audio Sample Packet)
52:47	Reserved	Reserved (0)
55:53	Suppl_A_Type_1	Supplementary audio type (Subpacket 1 in MST Audio Sample Packet)
56	Suppl_A_Mixed_1	Mix of main audio components and a supplementary audio track (Subpacket 1 in MST Audio Sample Packet)
57	Suppl_A_Valid_1	Audio stream contains a supplementary audio track (Subpacket 1 in MST Audio Sample Packet)
59:58	Reserved	Reserved (0)
60	LC_Valid_1	Validity of Language_Code (Subpacket 1 in MST Audio Sample Packet)
84:61	Language_Code_1	Audio stream language (Subpacket 1 in MST Audio Sample Packet)
85	Multiview_Left_2	Left stereoscopic picture (Subpacket 2 in MST Audio Sample Packet)
86	Multiview_Right_2	Right stereoscopic picture (Subpacket 2 in MST Audio Sample Packet)

continued...

Bit-field	Name	Description
92:87	Reserved	Reserved (0)
95:93	Suppl_A_Type_2	Supplementary audio type (Subpacket 2 in MST Audio Sample Packet)
96	Suppl_A_Mixed_2	Mix of main audio components and a supplementary audio track (Subpacket 2 in MST Audio Sample Packet)
97	Suppl_A_Valid_2	Audio stream contains a supplementary audio track (Subpacket 2 in MST Audio Sample Packet)
99:98	Reserved	Reserved (0)
100	LC_Valid_2	Validity of Language_Code (Subpacket 2 in MST Audio Sample Packet)
124:101	Language_Code_2	Audio stream language (Subpacket 2 in MST Audio Sample Packet)
125	Multiview_Left_3	Left stereoscopic picture (Subpacket 3 in MST Audio Sample Packet)
126	Multiview_Right_3	Right stereoscopic picture (Subpacket 3 in MST Audio Sample Packet)
132:127	Reserved	Reserved (0)
135:133	Suppl_A_Type_3	Supplementary audio type (Subpacket 3 in MST Audio Sample Packet)
136	Suppl_A_Mixed_3	Mix of main audio components and a supplementary audio track (Subpacket 3 in MST Audio Sample Packet)
137	Suppl_A_Valid_3	Audio stream contains a supplementary audio track (Subpacket 3 in MST Audio Sample Packet)
139:138	Reserved	Reserved (0)
140	LC_Valid_3	Validity of Language_Code (Subpacket 3 in MST Audio Sample Packet)
164:141	Language_Code_3	Audio stream language (Subpacket 3 in MST Audio Sample Packet)

5.2. Source Interfaces

The table lists the source's port interfaces.

Table 27. Source Interfaces

N is the number of symbols per clock.

Interface	Port Type	Clock Domain	Port	Direction	Description
Reset	Reset	N/A	`reset`	Input	Main asynchronous reset input.
Clock	Clock	N/A	`ls_clk`	Input	Link speed clock input. Relationship to `vid_clk` as a function of color depth: • 8 bpc: 1x vid_clk • 10 bpc: 1.25x vid_clk • 12 bpc: 1.5x vid_clk • 16 bpc: 2x vid_clk This signal connects to the transceiver output clock only if an application does

continued...

Interface	Port Type	Clock Domain	Port	Direction	Description
					not require low TMDS Bit Rate (below the minimum transceiver data rate), which means no oversampling is required. This signal should connect to a PLL output clock that meets the `vid_clk` relationship if an application requires low TMDS Bit Rate (below the minimum transceiver data rate), which means oversampling is required. Refer to Source Clock Tree on page 58 for more information.
	Clock	N/A	`vid_clk`	Input	Video data clock input. For RGB and YCbCr 4:4:4/4:2:2 transport: • 1 symbol per clock mode = pixel clock • 2 symbols per clock mode = pixel clock/2 • 4 symbols per clock mode = pixel clock/4 For YCbCr 4:2:0 transport: • 1 symbol per clock mode = pixel clock/2 • 2 symbols per clock mode = pixel clock/4 • 4 symbols per clock mode = pixel clock/8
	Clock	N/A	`audio_clk`	Input	Audio clock input. Connect this signal to `ls_clk` by qualifying the slower frequency of `audio_data` with `audio_de`. If you connect this signal to a clock at actual audio sample frequency, you must tie `audio_de` to 1. For audio channels greater than 8, do not drive `audio_clk` at actual audio sample clock; instead drive `audio_clk` with `ls_clk` and qualify `audio_data` with `audio_de`. *Note:* Applicable only when you turn on the **Support auxiliary** and **Support audio** parameters.
Video Data Port	Conduit	`vid_clk`	`vid_data[N*48-1:0]`	Input	Video 48-bit pixel data input port.

continued...

Interface	Port Type	Clock Domain	Port	Direction	Description
					• In 2 symbols per clock (N=2) mode, this port accepts two 48-bit pixels per clock. • In 4 symbols per clock (N=4) mode, this port accepts four 48-bit pixels per clock.
	Conduit	`vid_clk`	`vid_de[N-1:0]`	Input	Video data enable input that indicates active picture region.
	Conduit	`vid_clk`	`vid_hsync[N-1:0]`	Input	Video horizontal sync input.
	Conduit	`vid_clk`	`vid_vsync[N-1:0]`	Input	Video vertical sync input.
TMDS Data Port [4]	Conduit	`ls_clk`	`out_b[N*10-1:0]`	Output	TMDS encoded blue channel (0) output.
	Conduit	`ls_clk`	`out_g[N*10-1:0]`	Output	TMDS encoded green channel (1) output.
	Conduit	`ls_clk`	`out_r[N*10-1:0]`	Output	TMDS encoded red channel (2) output.
	Conduit	`ls_clk`	`out_c[N*10-1:0]`	Output	Clock channel output. For `out_c` values, refer to Table 28 on page 57 and Table 29 on page 58.
Encoder Control Port	Conduit	`ls_clk`	`mode`	Input	Encoding mode input. • 0: DVI • 1: HDMI
	Conduit	`ls_clk`	`TMDS_Bit_clock_Ratio`	Input	Indicates if TMDS Bit Rate is greater than 3.4Gbps. • 0: (TMDS Bit Rate) / (TMDS Clock Rate) ratio is 10 • 1 = (TMDS Bit Rate) / (TMDS Clock Rate) ratio is 40
	Conduit	`ls_clk`	`Scrambler_Enable`	Input	Enables scrambling. • 0: Instructs the source device not to perform scrambling • 1: Instructs the source device to perform scrambling
	Conduit	`ls_clk`	`ctrl[N*6-1:0]`	Input	DVI control side-band inputs to override the necessary control and synchronization data in the green and red channels.

continued...

(4) Connect to the transceiver data input if no oversampling is required. If oversampling is required, the port should connect to a DCFIFO and an oversampling user logic before connecting to a transceiver data input. Refer to Source Clock Tree on page 58 for more information.

Interface	Port Type	Clock Domain	Port	Direction	Description	
					Bit-Field	**Name**
					N*6+5	CTL3
					N*6+4	CTL2
					N*6+3	CTL1
					N*6+2	CTL0
					N*6+1	Reserved (0)
					N*6	Reserved (0)
					Refer to the *HDMI 1.4b Specification* for more information.	
Auxiliary Data Port (Applicable only when you enable **Support auxiliary** parameter)	Conduit	`ls_clk`	`aux_ready`	Output	Auxiliary data channel ready output. Asserted high to indicate that the core is ready to accept data.	
	Conduit	`ls_clk`	`aux_valid`	Input	Auxiliary data channel valid input to qualify the data.	
	Conduit	`ls_clk`	`aux_data[71:0]`	Input	Auxiliary data channel data input. For information about the bit-fields, refer to Figure 18 on page 43.	
	Conduit	`ls_clk`	`aux_sop`	Input	Auxiliary data channel start-of-packet input to mark the beginning of a packet.	
	Conduit	`ls_clk`	`aux_eop`	Input	Auxiliary data channel end-of-packet input to mark the end of a packet.	
Auxiliary Control Port (Applicable only when you enable **Support auxiliary** parameter)	Conduit	`ls_clk`	`gcp[5:0]`	Input	General Control Packet user input. For information about the bit-fields, refer to Table 19 on page 45.	
	Conduit	`ls_clk`	`info_avi[112:0]`	Input	Auxiliary Video Information InfoFrame user input. For information about the bit-fields, refer to Table 20 on page 46.	
	Conduit	`ls_clk`	`info_vsi[61:0]`	Input	Vendor Specific Information InfoFrame user input. For information about the bit-fields, refer to Table 21 on page 47.	
Audio Port (Applicable only when you enable **Support auxiliary** and	Conduit	`audio_clk`	`audio_CTS[19:0]`	Input	Audio CTS value input.	
	Conduit	`audio_clk`	`audio_N[19:0]`	Input	Audio N value input.	
	Conduit	`audio_clk`	`audio_data[255:0]`	Input	Audio data input. For audio channel values, refer to Table 30 on page 58.	

continued...

Interface	Port Type	Clock Domain	Port	Direction	Description
Support audio parameters)	Conduit	`audio_clk`	`audio_de`	Input	Audio data valid input.
	Conduit	`audio_clk`	`audio_mute`	Input	Audio mute input. No audio will be transmitted when this signal is asserted high.
	Conduit	`ls_clk`	`audio_info_ai[48:0]`	Input	Audio InfoFrame user input. *Note:* If you provide `audio_info_ai[48:0]` using `audio_clk` with actual audio sample frequency, you must synchronize the clock domain to `ls_clk` externally. For information about the bit-fields, refer to Table 23 on page 50.
	Conduit	`ls_clk`	`audio_metadata[165:0]`	Input	Carries additional information related to 3D audio and MST audio. *Note:* If you provide `audio_metadata[165:0]` using `audio_clk` with actual audio sample frequency, you must synchronize the clock domain to `ls_clk` externally. For information about the bit-fields, refer to Table 24 on page 51, Table 25 on page 51, and Table 26 on page 52.
	Conduit	`audio_clk`	`audio_format[4:0]`	Input	Controls the transmission of the 3D audio and indicates the audio format to be transmitted. **Bit-Field** — **Description** 4 — Assert to indicate the first 8 channels of each 3D audio sample. 3:0 — For information about the bit-fields, refer to Table 22 on page 48.

Table 28. out_c Value for TMDS Bit Rate Less than 3.4 Gbps

`TMDS_Bit_clock_Ratio` = 0 and `out_c` value is constant.

N	out_c Value
1	10'b1111100000
2	20'b1111100000_1111100000
4	40'b1111100000_1111100000 1111100000_1111100000

Table 29. out_c Value for TMDS Bit Rate Greater than 3.4 Gbps

`TMDS_Bit_clock_Ratio` = 1 and `out_c` value is repeated indefinitely.

N	out_c Value			
	t	t+1	t+2	t+3
1	10'h000	10'h000	10'h3ff	10'h3ff
2	20'h00000	20'hfffff	20'h00000	20'hfffff
4	40'hfffff 00000	40'hfffff 00000	40'hfffff 00000	40'hfffff 00000

Table 30. Audio Channel

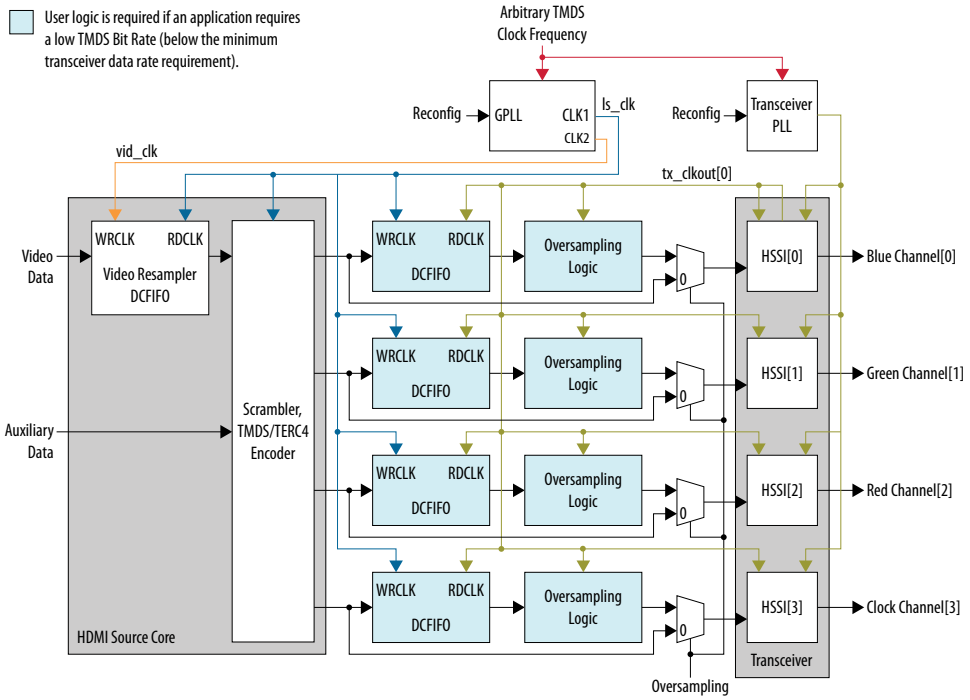
Bit-Field	Audio Channel	
	LPCM and 3D Audio (LPCM)	MST Audio (LPCM)
255:224	8 or 16 or 24 or 32	Stream 4 right channel
223:192	7 or 15 or 23 or 31	Stream 4 left channel
191:160	6 or 14 or 22 or 30	Stream 3 right channel
159:128	5 or 13 or 21 or 29	Stream 3 left channel
127:96	4 or 12 or 20 or 28	Stream 2 right channel
95:64	3 or 11 or 19 or 27	Stream 2 left channel
63:32	2 or 10 or 18 or 26	Stream 1 right channel
31:0	1 or 9 or 17 or 25	Stream 1 left channel

5.3. Source Clock Tree

The source uses various clocks.

Figure 23. Source Clock Tree

The figure shows how the different clocks connect in the source core.



For HDMI source, you must instantiate 4 transceiver channels: 3 channels to transmit data and 1 channel to transmit clock information.

The core uses a general purpose phase-locked loop (GPLL), that is referenced by an arbitrary TMDS clock frequency, to generate the link speed clock (`ls_clk`) and video clock (`vid_clk`).

- The video data clocks into the core at `vid_clk`.
- The TMDS data clocks out from the core at `ls_clk`.

The same arbitrary TMDS clock frequency is also used to drive the transceiver PLL. `ls_clk` and `tx_clkout[0]` are derived from `vid_clk` based on the color depth, TMDS_Bit_clock_Ratio, and user oversampling control bit information.

If an application requires low TMDS Bit Rate (below the transceiver minimum data rate requirement), then the application needs a user logic consisting of a DCFIFO and oversampling logic.

- The DCFIFO synchronizes the TMDS data from `ls_clk` to a faster transceiver output clock (`tx_clkout[0]`).
- The oversampling logic repeats each bit of the TMDS data a given number of times.
- When you enable the oversampling control bit, the transceiver transmits the TMDS data between the HDMI source core and the oversampling logic.
- You can use `tx_clkout[0]` across 4 channels if the transceiver is in bonding mode.

If an application does not require low TMDS Bit Rate, you can connect the core output directly to the transceiver with `tx_clkout[0]` driving the core `ls_clk`. You do not require the GPLL to generate `CLK1` (`ls_clk`).

Related Information

- HDMI Hardware Design Examples for Arria V and Stratix V Devices on page 17
- HDMI Hardware Design Examples for Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10 Devices on page 17

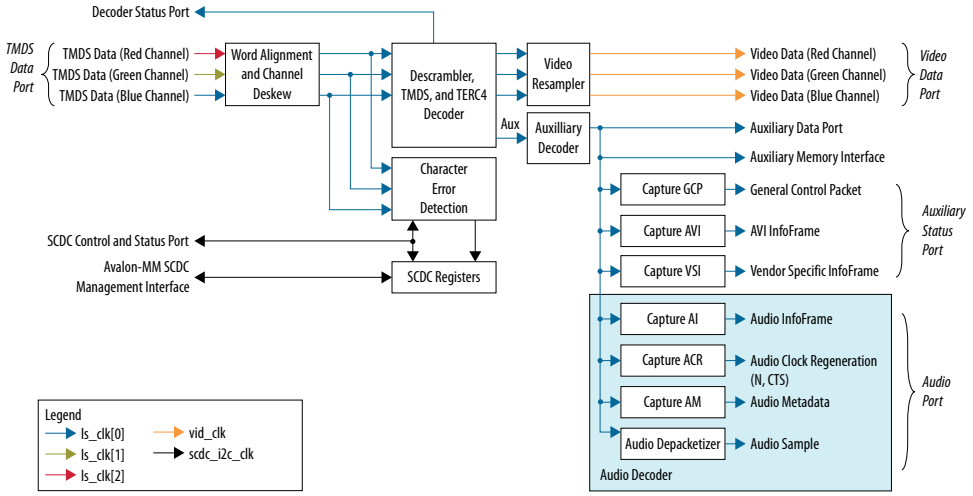
6. HDMI Sink

6.1. Sink Functional Description

The HDMI sink core provides direct connection to the Transceiver Native PHY through a 10-bit, 20-bit, or 40-bit parallel data path.

Figure 24. HDMI Sink Signal Flow Diagram

The figure below shows the flow of the HDMI sink signals. The figure shows the various clocking domains used within the core.



The sink core provides three 10-bit, 20-bit, or 40-bit data input paths corresponding to the color channels. The sink core clocks the three 10-bit, 20-bit, or 40-bit channels from the transceiver outputs using the respective transceiver clock outputs.

- Blue channel: 0
- Green channel: 1
- Red channel: 2

6.1.1. Sink Word Alignment and Channel Deskew

The input stage of the sink is responsible for synchronizing the incoming parallel data channels correctly. The synchronization is split to two stages: word alignment and channel deskew.

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

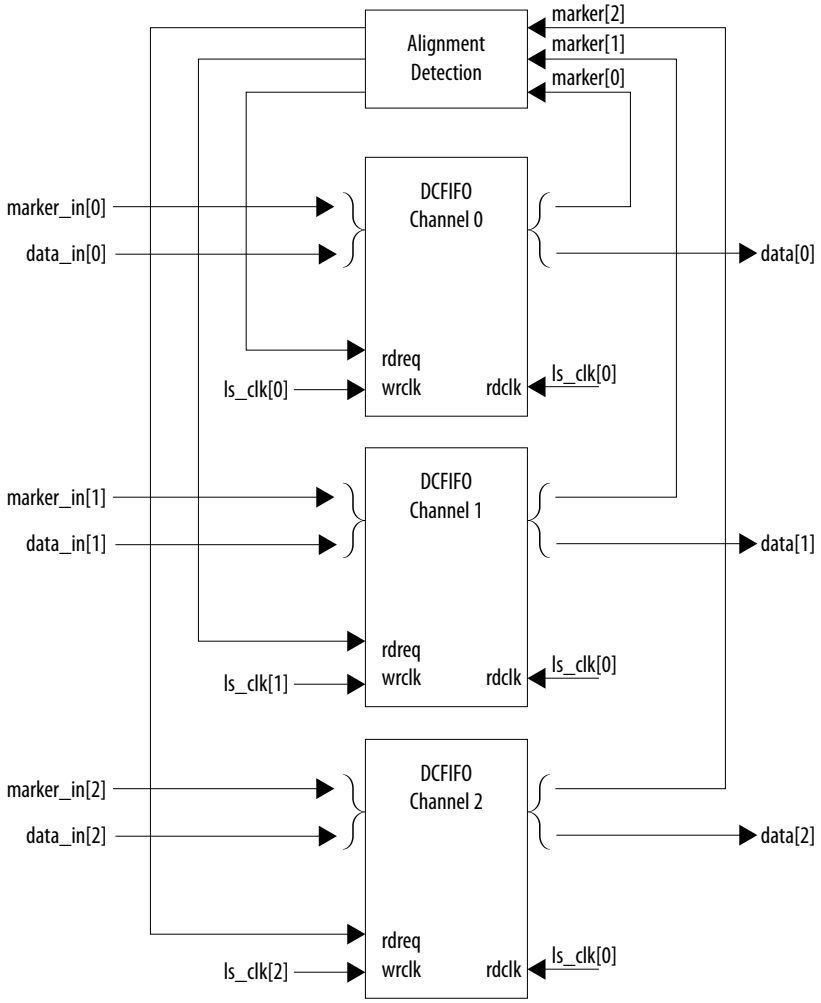
ISO 9001:2015 Registered

Table 31. Synchronization Stages

Stage	Description
Word Alignment	• Correctly aligns the incoming parallel data to word boundaries using bit-slip technique. • TMDS encoding does not guarantee unique control codes, but the core can still use the sequence of continuous symbols found in data and video preambles to align. • The alignment algorithm searches for 8 consecutive 0×54 or 0×ab corresponding to the data and video preambles. *Note:* The preambles are also present in Digital Video Interface (DVI) coding. • The alignment logic asserts a marker indicator when the 8 consecutive signals are detected. • Similarly, the logic infers alignment loss when 8K symbol clocks elapse without a single marker assertion. *Note:* If you are using Intel Arria 10 or Intel Cyclone 10 GX devices, soft word alignment logic in the HDMI RX core is disabled for HDMI 2.0 resolution (data rate >3.4 Gbps). Hard transceiver PCS word alignment is used with some control logic to achieve faster word alignment with more optimized resource utilization. Refer to the design example user guides for more information. *Note:* If you are using Intel Stratix 10 devices, the HDMI RX core uses a new word alignment algorithm logic to achieve fast word alignment time for HDMI 2.0 resolution (data rate >3.4Gbps).
Channel Deskew	• When the data channels are aligned, the core then attempts to deskew each channel. • The sink core deskews at the rising edge of the marker insertion. • For every correct deskewed lane, the marker insertion will appear in all three TMDS encoded streams. • The sink core deskews using three dual-clock FIFOs. • The dual-clock FIFOs also synchronize all three data streams to the blue channel clock to be used later throughout the decoder core.

Figure 25. Channel Deskew DCFIFO Arrangement

The figure below shows the signal flow diagram of the deskew logic.



The FIFO read signal of the channels is normally asserted. The sink core deasserts a particular FIFO read signal if a marker appears at its output and not in the other two FIFO outputs. By deasserting, the sink core stalls the data stream for sufficient cycles to remove the channel skew. If any of the FIFO channels overflow, the sink core asserts a reset signal which propagates backwards to the word alignment logic.

6.1.2. Sink Descrambler, TMDS/TERC4 Decoder

The sink TMDS/TERC4 decoder follows the HDMI/DVI specification. The core enable descrambling automatically when it detects the `Scramble_Enable` bit of the SCDC registers.

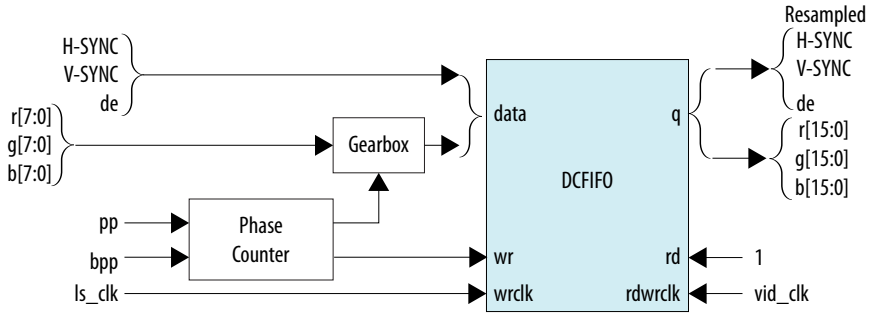
The sink core feeds the aligned channels into the TMDS/TERC4 decoder. You can parameterize the decoder to operate in 1, 2, or 4 TMDS symbols per clock. If you choose 2 or 4 TMDS symbols per clock, the decoder will produce 2 or 4 decoded symbols per clock. The decoded symbols per clock output supports high pixel clock resolutions on low-end FPGA devices.

6.1.3. Sink Video Resampler

The video resampler consists of a gearbox and a dual-clock FIFO (DCFIFO).

The gearbox converts 8-bpc data to 8-, 10-, 12- or 16-bpc data based on the current color depth. The GCP conveys the color depth (bpp) information.

Figure 26. Sink Resampler Signal Flow Diagram



The resampler adheres to the recommended phase count method described in *HDMI 1.4b Specification Section 6.5*.

- To keep the source and sink resamples synchronized, the source must send the packing-phase (pp) value to the sink during the vertical blanking phase, using the general control packet.
- The pp corresponds to the phase of the last pixel in the last active video line.
- The phase-counter logic compares its own pp value to the pp value received in the general control packet and *slips* the phase count if the two pp values do not agree.

The output from the resampler is fixed at 16 bpc. When the resampler operates in lower color depths, the low order bits are zero. The pixel data output format across color space are are described in Figure 10-12.

6.1.4. Sink Auxiliary Decoder

The sink core decodes the auxiliary data path into a 72-bit wide standard packet stream. The stream contains a valid, start-of-packet (SOP) and end-of-packet (EOP) marker.

Table 32. Auxiliary Packet Memory Map

This table lists the addresses corresponding to the captured packets.

Memory Start Address	Packet Name
0	NULL PACKET
4	Audio Clock Regeneration (N/CTS)
8	Audio Sample
12	General Control
16	ACP Packet

continued...

Memory Start Address	Packet Name
20	ISRC1 Packet
24	ISRC2 Packet
28	One Bit Audio Sample Packet 5.3.9
32	DST Audio Packet
36	High Bit rate (HBR) Audio Stream Packet
40	Gamut Metadata Packet
44	3D Audio Sample Packet
48	One Bit 3D Audio Sample Packet
52	Audio Metadata Packet
56	Multi-Stream Audio Sample Packet
60	One Bit Multi-Stream Audio Sample Packet
64	Vendor-Specific InfoFrame
68	AVI InfoFrame
72	Source Product Descriptor InfoFrame
76	Audio InfoFrame
80	MPEG Source InfoFrame
84	TSC VBI InfoFrame
88	Dynamic Range and Mastering InfoFrame

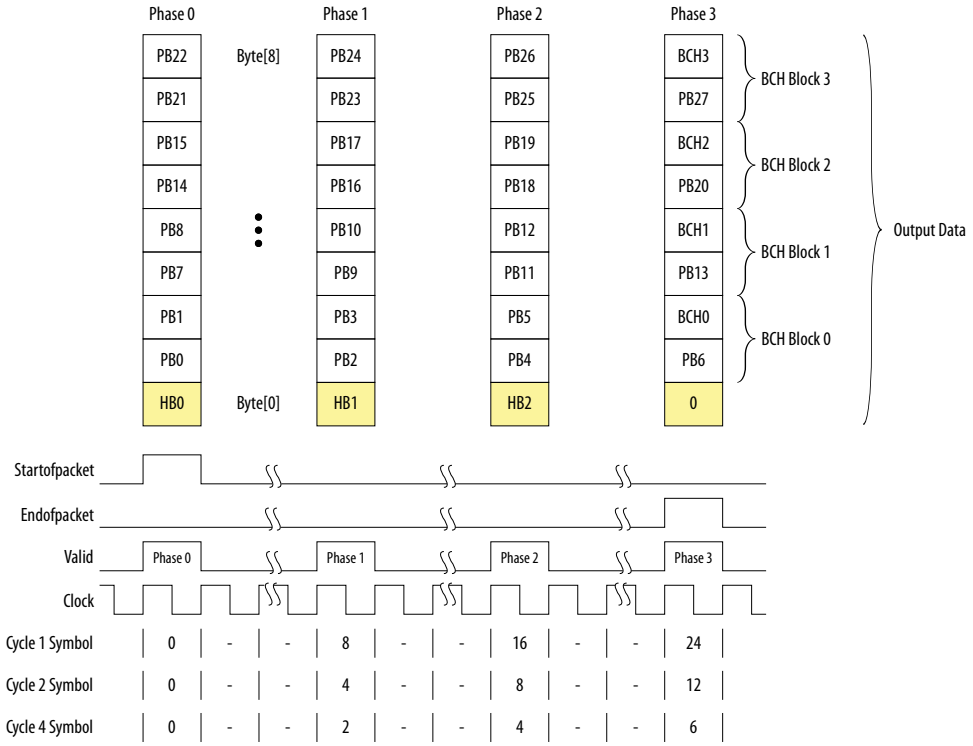
Table 33. Packet Payload Data Byte

This table shows the representation of each packet payload data byte.

Word Offset	Byte Offset								
	8	7	6	5	4	3	2	1	0
0	PB22	PB21	PB15	PB14	PB8	PB7	PB1	PB0	HB0
1	PB24	PB23	PB17	PB16	PB10	PB9	PB3	PB2	HB1
2	PB26	PB25	PB19	PB18	PB12	PB11	PB5	PB4	HB2
3	BCH3	PB27	BCH2	PB20	BCH1	PB13	BCH0	PB6	HBCH0

Figure 27. Auxiliary Data Stream Signal

The figure below shows the relationship between the data bit-field and its clock cycle based on 1-, 2-, or 4-symbol per clock mode.



The data output at EOP contains the received BCH error correcting code. The sink core does not perform any error correction within the core. The auxiliary data is available outside the core.

Note: You can find the bit-field nomenclature in the *HDMI 2.0b Specification*.

6.1.5. Sink Auxiliary Packet Capture

To simplify user applications and minimize external logic, the core captures 3 different packet types and presents the packets outside the core.

These packets are: General Control Packet (GCP), Auxiliary Video Information (AVI) InfoFrame, and HDMI Vendor Specific InfoFrame (VSI).

The GCP, AVI and VSI bit-fields (excluding control bit) are defined in Table 19 on page 45. Table 20 on page 46. and Table 21 on page 47 respectively with reserved bits return 0.

6.1.6. Sink Auxiliary Data Port

The auxiliary port is attached to external memory. This port allows you to write packets to memory for use outside the HDMI core.

The core calculates the address for the data port using the header byte of the received packet. The core writes packet types 0–15 into a contiguous memory region.

Figure 28. Typical Application of AUX Packet Register Interface

The figure below shows a typical application of the auxiliary data port.

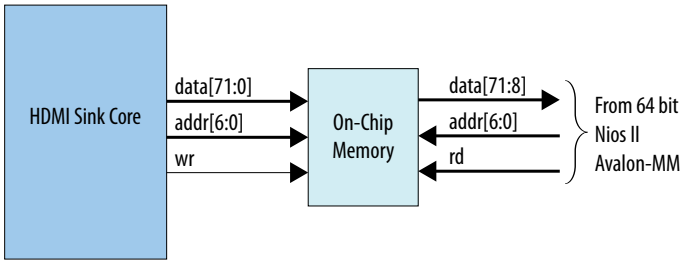


Table 34. Auxiliary Packet Memory Map

Memory Start Address	Packet Name
0	NULL PACKET
4	Audio Clock Regeneration (N/CTS)
8	Audio Sample
12	General Control
16	ACP Packet
20	ISRC1 Packet
24	ISRC2 Packet
28	One Bit Audio Sample Packet 5.3.9
32	DST Audio Packet
36	High Bitrate (HBR) Audio Stream Packet
40	Gamut Metadata Packet
44	3D Audio Sample Packet
48	One Bit 3D Audio Sample Packet
52	Audio Metadata Packet
56	Multi-Stream Audio Sample Packet
60	One Bit Multi-Stream Audio Sample Packet
64	Vendor-Specific InfoFrame
68	AVI InfoFrame
72	Source Product Descriptor InfoFrame
76	Audio InfoFrame
80	MPEG Source InfoFrame
84	TSC VBI InfoFrame
88	Dynamic Range and Mastering InfoFrame

Table 35. Packet Payload Data Byte

The table below lists the representation of each packet payload data byte.

Word Offset	Byte Offset								
	8	7	6	5	4	3	2	1	0
0	PB22	PB21	PB15	PB14	PB8	PB7	PB1	PB0	HB0
1	PB24	PB23	PB17	PB16	PB10	PB9	PB3	PB2	HB1
2	PB26	PB25	PB19	PB18	PB12	PB11	PB5	PB4	HB2
3	BCH3	PB27	BCH2	PB20	BCH1	PB13	BCH0	PB6	HBCH0

Note: The packet fields (PB0-PB26) are described in the HDMI 1.4b Specification (Chapter 8.2.1).

6.1.7. Sink Audio Decoder

The Audio Clock Regeneration packet transmits the CTS and N values required to synthesize the audio sample clock. The core also makes the CTS and N values available outside the core.

An audio clock synthesizer uses a phase-counter to recover the audio sample rate. The output from the audio clock synthesizer generates a valid pulse at the same rate as the audio sample clock from the attached source device. This valid pulse is available outside the core as an audio sample valid signal. This signal reads from a FIFO, which governs the rate of audio samples. The audio depacketizer drives the input to the FIFO.

The audio depacketizer extracts the 32-bit audio sample data from the incoming Audio Sample packets. The Audio Sample packets can hold from one to four sample data values. The audio format indicates the format of the received audio data as defined in Table 22 on page 48.

The Audio InfoFrame and Audio Metadata packets are not used within the core. The packets are captured and presented outside the core. The bit fields (excluding control bit) are defined in Table 23 on page 50, Table 24 on page 51, Table 25 on page 51, and Table 26 on page 52 with reserved bits return 0.

6.1.8. Status and Control Data Channel (SCDC) Interface

For applications using the HDMI 2.0b feature, the core provides a memory slave port to the SCDC registers.

This memory slave port connects to an I^2C slave component. The `TMDS_Bit_clock_Ratio` output from the SCDC interface indicates when the core requires the TMDS Bit Rate/TMDS Clock Rate ratio of 40. This bit is also stored in its corresponding field in the SCDC registers.

The *HDMI 2.0b Specification* requires the core to respond to the presence of the 5V input from the connector and the state of the HPD signal. The 5V input and HPD signal are used in the register mechanism updates. The signals are synchronous to the `scdc_i2c_clk` clock domain. You must create a 100-ms delay on the HPD signal externally to the core.

For more information about the Status and Control Data Channel, you may refer to *HDMI 2.0b Specification Chapter 10.4*. You can obtain the address map for the registers in the *HDMI 2.0b Specification*.

6.2. Sink Interfaces

The table lists the sink's port interfaces.

Table 36. Sink Interfaces

N is the number of symbols per clock.

Interface	Port Type	Clock Domain	Port	Direction	Description
Reset	Reset	N/A	`reset`	Input	Main asynchronous reset input. *Note:* Asserting the reset input resets the SCDC register.
Clock	Clock	N/A	`ls_clk[2:0]`	Input	Link speed clock input. These clocks correspond to the `in_r` (2), `in_g` (1), and `in_b` (0) TMDS encoded data inputs. Relationship to `vid_clk` as a function of color depth: • 8 bpc: 1x vid_clk • 10 bpc: 1.25x vid_clk • 12 bpc: 1.5x vid_clk • 16 bpc: 2x vid_clk This signal connects to the transceiver output clock only if TMDS Bit Rate is above the minimum transceiver data rate, which means no oversampling is required. This signal should connect to a PLL output clock that meets the `vid_clk` relationship if TMDS Bit Rate is below the minimum transceiver data rate, which means oversampling is required.
	Clock	N/A	`vid_clk`	Input	Video data clock input. For RGB and YCbCr 4:4:4/4:2:2 transport: • 1 symbol per clock mode = pixel clock • 2 symbols per clock mode = pixel clock/2 • 4 symbols per clock mode = pixel clock/4

continued...

Interface	Port Type	Clock Domain	Port	Direction	Description
					For YCbCr 4:2:0 transport: • 1 symbol per clock mode = pixel clock/2 • 2 symbols per clock mode = pixel clock/4 • 4 symbols per clock mode = pixel clock/8
	Clock	N/A	`scdc_i2_clk`	Input	Avalon-MM SCDC Management Interface clock input.
Video Data Port	Conduit	`vid_clk`	`vid_data[N*48-1:0]`	Output	Video 48-bit pixel data output port. In 2 symbols per clock (N=2) mode, this port produces two 48-bit pixels per clock. In 4 symbols per clock (N=4) mode, this port produces four 48-bit pixels per clock.
	Conduit	`vid_clk`	`vid_de[N-1:0]`	Output	Video data enable output that indicates active picture region.
	Conduit	`vid_clk`	`vid_hsync[N-1:0]`	Output	Video horizontal sync output.
	Conduit	`vid_clk`	`vid_vsync[N-1:0]`	Output	Video vertical sync output.
	Conduit	`vid_clk`	`locked[2:0]`	Output	Asserted when the HDMI sink core receives eight continuous synchronization characters and all channels are deskewed properly. Indicates that the HDMI sink core is locked to the TMDS signals. Each bit represents a color channel. **Bit-Field** / **Channel** 0 / Blue (0) 1 / Green (1) 2 / Red (2)
	Conduit	`vid_clk`	`vid_lock`	Output	Asserted when the received video data is determined to be stable and repetitive.

continued...

Interface	Port Type	Clock Domain	Port	Direction	Description
					The IP detects HTotal, VTotal, HSync Width, VSync Width, HSync Polarity, and VSync Polarity. • If any of these parameters change across 2 frames, the `vid lock` signal will deassert. • If any of these parameters are consistent for two frames, the IP asserts the `vid_lock` signal.
TMDS Data Port [5]	Conduit	`ls_clk[0]`	`in_b[N*10-1:0]`	Input	TMDS encoded blue channel (0) input.
	Conduit	`ls_clk[1]`	`in_g[N*10-1:0]`	Input	TMDS encoded green channel (1) input.
	Conduit	`ls_clk[2]`	`in_r[N*10-1:0]`	Input	TMDS encoded red channel (2) input.
	Conduit	`ls_clk[2:0]`	`in_lock[2:0]`	Input	Ready signal from the transceiver reset controller that indicates the transceivers are locked. Indicates the readiness of the up-stream block for the HDMI sink core to start operating. When this port is low, all blocks, except the SCDC registers and the character error detection block are hold in reset. Each bit represents a color channel. **Bit-Field** / **Channel** 0 / Blue (0) 1 / Green (1) 2 / Red (2)
Decoder Status Port	Conduit	`ls_clk[0]`	`ctrl[N*6-1:0]`	Output	DVI (mode = 0) status signals that overwrites the control and synchronization character in the green and red channels. **Bit-Field** / **Name** N*6+5 / CTL3

continued...

[5] Connect to the transceiver data output if no oversampling is required. If oversampling is required, the port should connect to a DCFIFO and an oversampling user logic before connecting to a transceiver data output. Refer to Sink Clock Tree on page 74 for more information.

Interface	Port Type	Clock Domain	Port	Direction	Description	
					N*6+4	CTL2
					N*6+3	CTL1
					N*6+2	CTL0
					N*6+1	Reserved (0)
					N*6	Reserved (0)
					Refer to the *HDMI 1.4b Specification* for more information.	
	Conduit	`ls_clk[0]`	`mode`	Output	Indicates the encoding mode of the incoming TMDS signals. • 0: DVI • 1: HDMI	
SCDC Control Port	Conduit	`scdc_i2c_clk`	`in_5v_power`	Input	Detects the presence of 5V input voltage.	
	Conduit	`scdc_i2c_clk`	`in_hpd`	Input	Detects the Hot Plug Detect (HPD) status.	
	Conduit	`scdc_i2c_clk`	`TMDS_Bit_clock_Ratio`	Output	Indicates if TMDS Bit Rate is greater than 3.4Gbps • 0: (TMDS Bit Rate) / (TMDS Clock Rate) ratio is 10 • 1: (TMDS Bit Rate) / (TMDS Clock Rate) ratio is 40	
Avalon-MM SCDC Management Interface [6]	Avalon-MM	`scdc_i2c_clk`	`scdc_i2c_addr[7:0]`	Input	Address.	
	Avalon-MM	`scdc_i2c_clk`	`scdc_i2c_r`	Input	Assert to indicate a read transfer.	
	Avalon-MM	`scdc_i2c_clk`	`scdc_i2c_rdata[7:0]`	Output	Data driven from the core in response to a read transfer.	
	Avalon-MM	`scdc_i2c_clk`	`scdc_i2c_w`	Input	Assert to indicate a write transfer.	
	Avalon-MM	`scdc_i2c_clk`	`scdc_i2c_wdata[7:0]`	Input	Data for write transfers.	
Auxiliary Data Port (Applicable only when you enable **Support auxiliary** parameter)	Conduit	`ls_clk[0]`	`aux_valid`	Output	Auxiliary data channel valid output to qualify the data.	
	Conduit	`ls_clk[0]`	`aux_data[71:0]`	Output	Auxiliary data channel data output. For information about the bit-fields, refer to Figure 27 on page 66.	

continued...

[6] Refer to *HDMI 2.0b Specification Section 10.4* for address and data bit mapping.

Interface	Port Type	Clock Domain	Port	Direction	Description
	Conduit	`ls_clk[0]`	`aux_sop`	Output	Auxiliary data channel start-of-packet output to mark the beginning of a packet.
	Conduit	`ls_clk[0]`	`aux_eop`	Output	Auxiliary data channel end-of-packet output to mark the end of a packet.
	Conduit	`ls_clk[0]`	`aux_error`	Output	Asserted when there is auxiliary data channel CRC error.
Auxiliary Status Port (Applicable only when you enable **Support auxiliary** parameter)	Conduit	`ls_clk[0]`	`gcp[5:0]`	Output	General Control Packet output. For information about the bit-fields, refer to Table 19 on page 45.
	Conduit	`ls_clk[0]`	`info_avi[111:0]`	Output	Auxiliary Video Information InfoFrame output. For information about the bit-fields, refer to Table 20 on page 46.
	Conduit	`ls_clk[0]`	`info_vsi[60:0]`	Output	Vendor Specific Information InfoFrame output. For information about the bit-fields, refer to Table 21 on page 47.
Auxiliary Memory Interface (Applicable only when you enable **Support auxiliary** parameter)	Conduit	`ls_clk[0]`	`aux_pkt_addr[6:0]`	Output	Auxiliary packet memory buffer address output.
	Conduit	`ls_clk[0]`	`aux_pkt_data[71:0]`	Output	Auxiliary packet memory buffer data output.
	Conduit	`ls_clk[0]`	`aux_pkt_wr`	Output	Auxiliary packet memory buffer write strobe output.
Audio Port (Applicable only when you enable **Support auxiliary** and **Support audio** parameters)	Conduit	`ls_clk[0]`	`audio_CTS[19:0]`	Output	Audio CTS value output.
	Conduit	`ls_clk[0]`	`audio_N[19:0]`	Output	Audio N value output.
	Conduit	`ls_clk[0]`	`audio_data[255:0]`	Output	Audio data output. For audio channel values, refer to Table 30 on page 58.
	Conduit	`ls_clk[0]`	`audio_de`	Output	Audio data valid output.
	Conduit	`ls_clk[0]`	`audio_metadata[164:0]`	Output	Additional information related to 3D audio and MST audio. For information about the bit-fields, refer to Table 24 on page 51, Table 25 on page 51, and Table 26 on page 52.
	Conduit	`ls_clk[0]`	`audio_format[4:0]`	Output	Indicates 3D audio status and the audio format detected.

continued...

Interface	Port Type	Clock Domain	Port	Direction	Description	
					Bit-Field	**Descriptio n**
					4	The core asserts to indicate the first 8 channels of each 3D audio sample.
					3:0	For information about the bit-fields, refer to Table 22 on page 48.
	Conduit	`ls_clk[0]`	`audio_info_ai[47:0]`	Output	Audio InfoFrame output bundle. For information about the bit-fields, refer to Table 23 on page 50.	

6.3. Sink Clock Tree

The sink core uses various clocks.

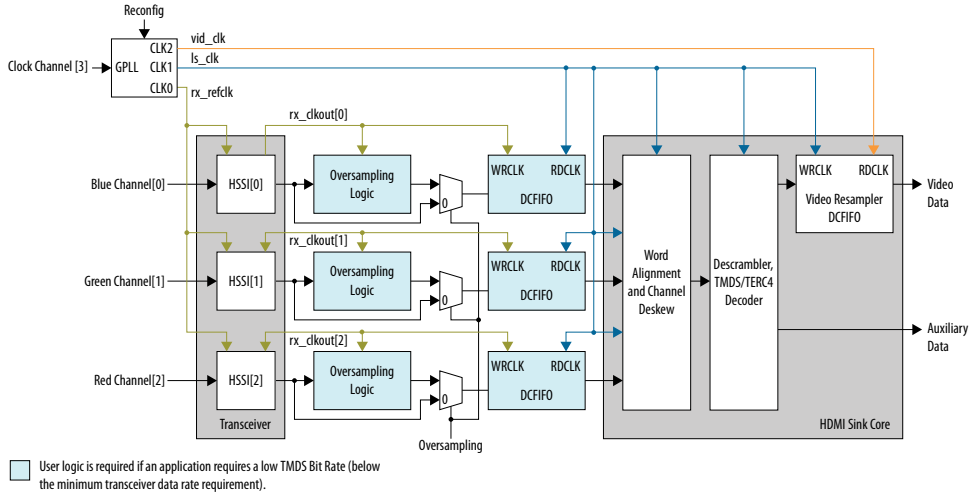
The logic clocks the transceiver data into the core using the three CDR clocks: (rx_clk[2:0]).

The TMDS and TERC4 decoding is done at the link-speed clock (`ls_clk`). The sink then resamples the pixel data and presents the data at the output of the core at the video pixel clock (`vid_clk`).

The pixel data clock depends on the video format used (within HDMI specification).

Figure 29. Sink Clock Tree

The figure shows how the different clocks connect in the sink core.



For HDMI sink, you must instantiate 3 receiver channels to receive TMS data.

The core uses a general purpose phase-locked loop (GPLL), that is referenced by the source Clock Channel, to generate the transceiver CDR reference clock (`rx_refclk`), link speed clock (`ls_clk`), and video clock (`vid_clk`) for the core.

Note: GPLL refers to IOPLL Intel FPGA IP for Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10 devices; PLL Intel FPGA IP for Arria V and Stratix V devices.

- The TMDS data clocks into the core at `ls_clk[2:0]` with all channels driven by the same clock source (`GPLL CLK1`).
- The video data clocks out from the core at `vid_clk`.

`rx_refclk`, `ls_clk`, and `vid_clk` are derived based on the color depth, TMDS_Bit_clock_Ratio, user oversampling control bit information, and the detected Clock Channel frequency band.

If an application requires low TMDS Bit Rate (below the transceiver minimum data rate requirement), then the application needs a user logic consisting of a DCFIFO and oversampling logic.

- The oversampling logic extracts the data from the oversampled incoming data stream.
- When you enable the oversampling control bit, the DCFIFO gets the TMDS data between the transceiver and the oversampling logic.
- The DCFIFO synchronizes the TMDS data from the fastest transceiver output clock (`rx_clkout[2:0]`) to the `ls_clk` domain.

If an application does not require low TMDS Bit Rate, the Clock Channel drives the transceiver `rx_refclk` directly. You can also connect the transceiver output to the core with `ls_clk[2:0]` driven by `rx_clkout[2:0]`.

Related Information

- HDMI Hardware Design Examples for Arria V and Stratix V Devices on page 17

- HDMI Hardware Design Examples for Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10 Devices on page 17

7. HDMI Parameters

Use the settings in the HDMI parameter editor to configure your design.

7.1. HDMI Source Parameters

Table 37. HDMI Source Parameters

Parameter	Value	Description
Device family	Intel Stratix 10 Intel Arria 10 Intel Cyclone 10 GX Arria V Stratix V	Targeted device family; matches the project device family.
Direction	Transmitter Receiver	Select HDMI transmitter.
Symbols per clock	1, 2, or 4 symbols per clock	Determines how many TMDS symbols and pixels are processed per clock. • Stratix V devices support 1 or 2 symbols per clock • Arria V devices support 1, 2, or 4 symbols per clock • Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10 devices support only 2 symbols per clock
Support auxiliary	0 = No AUX 1 = AUX	Determines if auxiliary channel encoding is included. This parameter is turned on by default.
Support deep color	0 = No deep color 1 = Deep color	Determines if the core can encode deep color formats. This parameter is turned on by default.
Support audio	0 = No audio 1 = Audio	Determines if the core can encode audio data. To enable this parameter, you must also enable the **Support auxiliary** parameter. This parameter is turned on by default.

7.2. HDMI Sink Parameters

Table 38. HDMI Sink Parameters

Parameter	Value	Description
Device family	Intel Stratix 10 Intel Arria 10 Intel Cyclone 10 GX Arria V	Targeted device family; matches the project device family.

continued...

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

Parameter	Value	Description
	Stratix V	
Direction	Transmitter Receiver	Select HDMI receiver.
Symbols per clock	1, 2, or 4 symbols per clock	Determines how many TMDS symbols and pixels are processed per clock. • Stratix V devices support 1 or 2 symbols per clock • Arria V devices support 1, 2, or 4 symbols per clock • Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10 devices support only 2 symbols per clock
Support auxiliary	0 = No AUX 1 = AUX	Determines if auxiliary channel encoding is included. This parameter is turned on by default.
Support deep color	0 = No deep color 1 = Deep color	Determines if the core can encode deep color formats. This parameter is turned on by default.
Support audio	0 = No audio 1 = Audio	Determines if the core can encode audio data. To enable this parameter, you must also enable the **Support auxiliary** parameter. This parameter is turned on by default.
Manufacturer OUI	—	The Manufacturer Organizationally Unique Identifier (OUI) assigned to the manufactured device to be written into the SCDC registers of address 0xD0, 0xD1, and 0xD2. Key in 3 byte hexadecimal data.
Device ID String	—	The Device Identification (ID) string to be written into the SCDC registers from addresses 0xD3 to 0xDa. Use this parameter to identify the sink device. You can key in up to eight ASCII characters. If you use less than eight characters, the unused bytes are set to 0x00.
Hardware Revision	—	Indicates the major and minor revisions of the hardware. Key in one byte of integer data. • Upper byte represents major revision. • Lower byte represents minor revision. The hardware major revision increments on a major silicon or board revision. The hardware minor revision increments on a minor silicon revision or minor board revision and resets to 0 when the major revision increments.

8. HDMI Simulation Example

The HDMI simulation example evaluates the functionality of the HDMI Intel FPGA IP core and provides a starting point for you to create your own simulation.

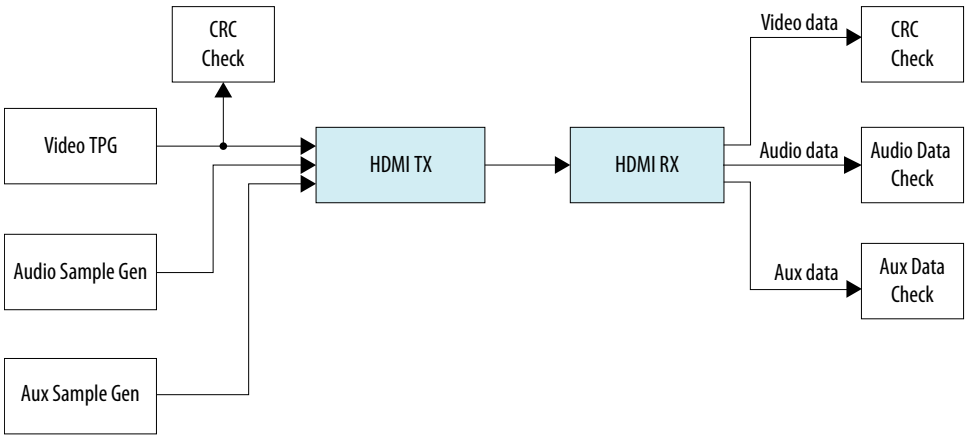
This simulation example targets the ModelSim - Intel FPGA Starter Edition simulator. The simulation covers the following core features:

- IEC-60958 audio format
- Standard H/V/DE/RGB input video format
- Support for 4 symbols per clock
- Support for HDMI 2.0b scrambled operation

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

Figure 30. HDMI Testbench



The Test Pattern Generator (TPG) provides the video stimulus. The IP core stimulates the HDMI TX core using an audio packet generator and aux packet generator. The output from the HDMI TX core drives the HDMI RX core.

The IP core requires a memory-mapped master stimulus to operate the testbench for HDMI 2.0b scrambling. This stimulus implements the activity normally seen across the I^2C DDC channel. At this point, the IP core asserts the scramble enable bit in the SCDC registers.

The testbench implements CRC checking on the input and output video. The testbench checks the CRC value of the transmitted data against the CRC calculated in the received video data. The testbench performs the checking after detecting 4 stable V-SYNC signals from the receiver.

The aux sample generator generates a fixed data to be transmitted from the transmitter. On the receiver side, the generator compares whether the expected aux data is received and decoded correctly.

The audio sample generator generates an incrementing test data pattern to be transmitted through the audio channel. On the receiver side, the audio data checker checks and compares whether the incrementing test data pattern is received and decoded correctly.

8.1. Simulation Walkthrough

Setting up and running the HDMI simulation example consists of two steps.

Note: This simulation flow applies only to Intel Quartus Prime Standard Edition using ModelSim - Intel FPGA Starter Edition. For Intel Quartus Prime Pro Edition flow, refer to the respective *Design Example User Guides*.

1. Copy the simulation files from `<IP root directory>/altera/altera_hdmi/sim_example` to your working directory.
2. Generate the IP simulation files and scripts, compile, and simulate.
   a. Start the Nios II Command Shell.
   b. Type the command below and enter.

```
sh runall.sh
```

This script executes the following commands:

Command	
Generate the simulation files for the HDMI cores.	• `ip-generate --project-directory=./ --component-file=./hdmi_rx_single.qsys --output-directory=./hdmi_rx_single/sim/ --file-set=SIM_VERILOG --report-file=sopcinfo:./hdmi_rx_single.sopcinfo --report-file=html:./hdmi_rx_single.html --report-file=spd:./hdmi_rx_single/sim/hdmi_rx_single.spd --report-file=qip:./hdmi_rx_single/sim/hdmi_rx_single.qip` • `ip-generate --project-directory=./ --component-file=./hdmi_rx_double.qsys --output-directory=./hdmi_rx_double/sim/ --file-set=SIM_VERILOG --report-file=sopcinfo:./hdmi_rx_double.sopcinfo --report-file=html:./hdmi_rx_double.html --report-file=spd:./hdmi_rx_double/sim/hdmi_rx_double.spd --report-file=qip:./hdmi_rx_double/sim/hdmi_rx_double.qip` • `ip-generate --project-directory=./ --component-file=./hdmi_tx_single.qsys --output-directory=./hdmi_tx_single/sim/ --file-set=SIM_VERILOG --report-file=sopcinfo:./hdmi_tx_single.sopcinfo --report-file=html:./hdmi_tx_single.html --report-file=spd:./hdmi_tx_single/sim/hdmi_tx_single.spd --report-file=qip:./hdmi_tx_single/sim/hdmi_tx_single.qip` • `ip-generate --project-directory=./ --component-file=./hdmi_tx_double.qsys --output-directory=./hdmi_tx_double/sim/ --file-set=SIM_VERILOG --report-file=sopcinfo:./hdmi_tx_double.sopcinfo --report-file=html:./hdmi_tx_double.html --report-file=spd:./hdmi_tx_double/sim/hdmi_tx_double.spd --report-file=qip:./hdmi_tx_double/sim/hdmi_tx_double.qip`
Merge the four resulting `msim_setup.tcl` scripts to create a single `mentor/msim_setup.tcl` script.	`ip-make-simscript --spd=./hdmi_tx_single/sim/hdmi_tx_single.spd --spd=./hdmi_tx_double/sim/hdmi_tx_double.spd --spd=./hdmi_rx_single/sim/hdmi_rx_single.spd --spd=./hdmi_rx_double/sim/hdmi_rx_double.spd`
Compile and simulate the design in the ModelSim software.	`vsim -c -do msim_hdmi.tcl`
Generate the simulation files for the HDMI cores.	
Merge the resulting `msim_setup.tcl` scripts to create a single `mentor/msim_setup.tcl` script.	
Compile and simulate the design in the ModelSim software.	

Example successful result:

```
# SYMBOLS_PER_CLOCK = 4
# VIC = 0
# AUDIO_CLK_DIVIDE = 800
# TEST_HDMI_6G = 1
# Simulation pass
# ** Note: $finish : bitec_hdmi_tb.v (647)
```

```
     Time: 15702552 ns Iteration: 3 Instance: /bitec_hdmi_tb
# End time: 14:39:02 on Feb 04,2016, Elapsed time: 0:03:17
# Errors: 0, Warnings: 134
```

9. HDMI Intel FPGA IP User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
18.1	HDMI Intel FPGA IP User Guide
18.0	HDMI Intel FPGA IP User Guide
17.1	HDMI IP Core User Guide
17.0	HDMI IP Core User Guide
16.1	HDMI IP Core User Guide
16.0	HDMI IP Core User Guide
15.1	HDMI IP Core User Guide
15.0	HDMI IP Core User Guide
14.1	HDMI IP Core User Guide

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

10. Document Revision History for the HDMI Intel FPGA IP User Guide

Document Version	Intel Quartus Prime Version	Changes
2019.04.29	19.1	• Added support for Intel Stratix 10 L-tile devices. Support for both Intel Stratix 10 L-tile and H-tile devices are final. • Updated the support for YCbCr 4:2:2 pixel encoding in the *Resource Utilization* section. The HDMI IP core supports 8-bit and 10-bit color depth for YCbCr 4:2:2 pixel encoding. • Added performance data for Intel Stratix 10 L-tile and H-tile devices, and updated the data for Intel Arria 10 and Intel Cyclone 10 GX devices for version 19.1. • Updated the description for the `locked[2:0]`, `in_lock[2:0]`, and `ctrl[N*6-1:0]` ports. • Added infomatition insertion and filtration for the control ports in the *Source Auxiliary Control Port* section.
2019.01.21	18.1	• Added a note in the *Sink Word Alignment and Channel Deskew* section that the word alignment logic in the HDMI RX core is disabled for HDMI 2.0 resolution (data rate >3.4 Gbps) in Intel Arria 10 and Intel Cyclone 10 GX devices. For Intel Stratix 10 devices, the HDMI RX core uses a new word alignment algorithm logic to achieve fast word alignment time for HDMI 2.0 resolution (data rate >3.4Gbps). • Updated the description for the `vid_lock` port to add that the IP detects HTotal, VTotal, HSync Width, VSync Width, HSync Polarity, and VSync Polarity. and a change in these parameters across two frames will deassert the `vid_lock` signal.
2018.05.07	18.0	• Update the HDMI specification reference to 2.0b. The HDMI Intel FPGA IP core now supports *HDMI Specification 2.0b*. • Added preliminary support for Intel Stratix 10 (H-Tile) devices. • Updated support for Intel Cyclone 10 GX devices to final. • Clarified in the features list that HDMI IP core supports up to 32 channels in 2-channel or 8-channel layouts. • Added link to the *HDMI Intel Cyclone 10 GX FPGA IP Design Example User Guide*. • Updated all IP names as part of standardization and rebranding exercise. • Removed a note that said the HDMI RX core does not support SCDC read request feature for this release. The HDMI RX core fully supports SCDC features since version 17.1. • Added a note in the *Sink Clock Tree* section that GPLL refers to IOPLL Intel FPGA IP for Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10 devices; PLL Intel FPGA IP for Arria V and Stratix V devices. • Edited the recommended speed grade information forIntel Cyclone 10 GX. The recommended speed grade is -5. • Edited typo in *3D Audio Input Example* figure. • Changed the term *Video Format* to *Pixel Encoding* to be consistent with *HDMI Specification 2.0b*. • Restructured the document. Placed the *HDMI Hardware Design* chapter after the *HDMI Getting Started* chapter.

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

Date	Version	Changes
November 2017	2017.11.06	• Added advance support for Intel Cyclone 10 GX devices. • Added resource utilization data for Intel Cyclone 10 GX devices. • Changed *bits per color (bpc)* to *bits per component (bpc)* as stated in the *HDMI Specification 2.0*. • Renamed HDMI IP core to HDMI Intel FPGA as per Intel rebranding. • Changed the term Qsys to Platform Designer. • Reorganized and updated the *Source Functional Description* and *Source Functional Description* sections for better understanding. • Added description for the following new bit-fields: — Audio InfoFrame Bundle Bit-fields — Audio Metadata Bundle Bit-Fields for Packet Header and Control — Audio Metadata Bundle Bit-Fields for Packet Content When 3D_AUDIO = 1 — Audio Metadata Bundle Bit-Fields for Packet Content When 3D_AUDIO = 0 • Added support for up to 32 audio channels. • Added support for up to 1,536 kHz audio sample frequency. • Updated the *3D Audio Format* section and the description for `audio_clk` that for audio channels greater than 8, do not drive `audio_clk` at actual audio sample clock. Instead drive `audio_clk` with `ls_clk` and qualify `audio_data` with `audio_de` • Updated the *HDMI Intel FPGA Source Clock Tree* and *HDMI Intel FPGA Sink Clock Tree* sections. • Updated the *HDMI Intel FPGA Source Parameter* and *HDMI Intel FPGA Sink Parameter* sections. • Updated the *HDMI Intel FPGA Source Interfaces* and *HDMI Intel FPGA Sink Interfaces* sections. • Updated the description for the **Support for deep color** parameter. The parameter is now turned on by default. • Edited the HDMI Intel FPGA testbench block diagram. Removed 4 symbols/clock to avoid confusion. • Added a note in the *HDMI Intel FPGA Hardware Demonstration* section that the demonstration is only applicable for Arria V and Stratix V devices. For Intel Arria 10 devices, refer to the *HDMI Intel FPGA Design Example User Guide for Intel Arria 10 Devices*. • Added a note in the *Simulation Walkthrough* section that the walkthrough is only applicable for Intel Quartus Prime Standard Edition. For Intel Quartus Prime Pro Edition, refer to the *HDMI Intel FPGA Design Example User Guide for Intel Arria 10 Devices*. • Moved information about the HDMI Intel FPGA design example parameters to the *HDMI Intel FPGA Design Example User Guide for Intel Arria 10 Devices*.
May 2017	2017.05.08	• Rebranded as Intel. • Added recommended speed grades for Intel Arria 10 devices.
December 2016	2016.12.20	• Updated the HDMI IP core resource utilization table with 16.1 information. • Added a note for YCbCr 4:2:2 video format that 8 and 10 bits per color use the same pixel encoding as 12 bits per color, but the valid bits are left-justified with zeros padding the bits below the least significant bit. • Added information for the new Design Example parameters. • Removed all Arria 10 design example related information. For more information about Arria 10 design examples, refer to the *HDMI IP Core Design Example User Guide*. • Edited the typos in the HDMI Audio Format topic. • Added information that the HDMI IP core does not support 8-channel audio. • Added a new output port `version[31:0]` for HDMI source and sink.

continued...

Date	Version	Changes
May 2016	2016.05.02	• Updated the HDMI IP core resource utilization table with 16.0 information. • Added information about Audio Metadata Packet for *HDMI Specification Version 2.0*. • Added information about new HDMI source ports: — `audio_metadata[164:0]` — `audio_format[4:0]` • Added information about new HDMI sink ports: — `audio_metadata[164:0]` — `audio_format[4:0]` — `vid_lock` — `aux_error` • Provided detailed information about the HDMI source and sink `audio_de[7:0]` port. • Updated the testbench diagram and description to include audio data and auxiliary data information. • Added a note for Altera PLL to place the PLL in the transmit path (`pll_hdmi_tx`) in the physical location next to the transceiver PLL. • Updated the HDMI sideband signals (HDMI AVI and VSI bit-fields) with default values. • Added links to archived versions of the *HDMI IP Core User Guide*.
November 2015	2015.11.02	• Updated the HDMI IP core resource utilization table with 15.1 information. • Changed instances of *Quartus II* to *Intel Quartus Prime*. • Added full support for Arria 10 devices. • Added support for new features: — Deep color — 8-channel audio • Added the following parameters for HDMI source: — **Support for 8-channel audio** — **Support for deep color** • Added the following parameters for HDMI sink: — **Support for 8-channel audio** — **Support for deep color** — **Manufacturer OUI** — **Device ID String** — **Hardware Revision** • Updated the following interface ports for HDMI source: — Added `ctrl` port — Removed `gcp_Set_AVMute` and `gcp_Clear_AVMute` ports • Updated the following interface ports for HDMI sink: — Added `ctrl` , `mode`, `in_5v_power`, and `in_hpd` ports — Removed `gcp_Set_AVMute` and `gcp_Clear_AVMute` ports • Updated the HDMI sink and source block diagrams to reflect the new features. • Provided block diagrams for deep color mapping. • Generalized the HDMI hardware demonstration design for all supported device families (Arria V, Stratix V, and Arria 10) with detailed description.
May 2015	2015.05.04	• Updated the HDMI IP core resource utilization table with 15.0 information. • Added information about 4 symbols per clock mode. • Added information about Status and Control Data Channel (SCDC) for *HDMI specification version 2.0*. • Added the following interface ports for HDMI source: — `TMDS_Bit_clock_Ratio` — `Scrambler_Enable`

continued...

Date	Version	Changes
		• Added the `TMDS_Bit_clock_Ratio` interface port for HDMI sink. • Updated the HDMI hardware demonstration design with HDMI 2.0 information. • Added software process flow for the HDMI hardware demonstration.
December 2014	2014.12.15	Initial release.