C2M0045170D

Silicon Carbide Power MOSFET
C2M^{TM} MOSFET Technology
N-Channel Enhancement Mode

Features

- 2nd generation SiC MOSFET technology
- High blocking voltage with low On-Resistance
- High speed switching with low capacitances
- Resistant to latch-up
- Halogen Free, RoHS Compliant

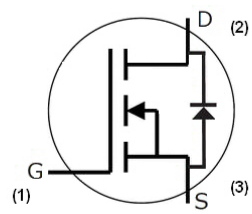
Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency

Applications

- Solar inverters
- Switch Mode Power Supplies
- High voltage DC/DC converters
- Motor drive
- Pulsed power applications

Package



Part Number	Package	Marking
C2M0045170D	TO-247-3L	C2M0045170D

Maximum Ratings (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1700	V	V_{GS} = 0 V, I_D = 100 μA	
V_{GSmax}	Gate - Source Voltage	-10/+25	V	Absolute maximum values, AC (f >1 Hz)	Note: 1
V_{GSop}	Gate - Source Voltage	-5/+20	V	Recommended operational values	Note: 2
I_D	Continuous Drain Current	75	A	V_{GS} =20 V, T_C = 25˚C	Fig. 19
		48		V_{GS} =20 V, T_C = 100˚C	
$I_{D(pulse)}$	Pulsed Drain Current	160	A	Pulse width t_P limited by T_{jmax}	Fig. 22
P_D	Power Dissipation	338	W	T_C=25˚C, T_J = 150 ˚C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-40 to +150	˚C		
T_L	Solder Temperature	260	˚C	1.6mm (0.063”) from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): When using MOSFET Body Diode V_{GSmax} = -5V/+25V
Note (2): MOSFET can also safely operate at 0/+20V

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1700			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	3.0	4	V	V_{DS} = V_{GS}, I_D = 18mA	Fig. 11
			2.5		V	V_{DS} = V_{GS}, I_D = 18mA, T_J = 150 °C	
I_{DSS}	Zero Gate Voltage Drain Current		2	100	μA	V_{DS} = 1700 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			600	nA	V_{GS} = 20 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		40	70	mΩ	V_{GS} = 20 V, I_D = 50 A	Fig. 4,5,6
			80			V_{GS} = 20 V, I_D = 50 A, T_J = 150 °C	
g_{fs}	Transconductance		24.7		S	V_{DS}= 20 V, I_{DS}= 50 A	Fig. 7
			23.4			V_{DS}= 20 V, I_{DS}= 50 A, T_J = 150 °C	
C_{iss}	Input Capacitance		3455		pF	V_{GS} = 0 V V_{DS} = 1200 V f = 1 MHz V_{AC} = 25 mV	Fig. 17,18
C_{oss}	Output Capacitance		171				
C_{rss}	Reverse Transfer Capacitance		6.7				
E_{oss}	C_{oss} Stored Energy		139		μJ		Fig 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		188		pF	V_{GS} = 0 V, V_{DS} = 0... 1200V	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		255		pF		
E_{ON}	Turn-On Switching Energy (SiC Diode FWD)		2.5		mJ	V_{DS} = 1200 V, V_{GS} = -5/20 V, I_D = 50A, $R_{G(ext)}$ = 2.5Ω, L= 99 μH, T_J = 150 °C, using SiC Diode as FWD	Fig. 26, 29b Note 2
E_{OFF}	Turn Off Switching Energy (SiC Diode FWD)		1.4				
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		4.9		mJ	V_{DS} = 1200 V, V_{GS} = -5/20 V, I_D = 50A, $R_{G(ext)}$ = 2.5Ω, L= 99 μH, T_J = 150 °C, using MOSFET as FWD	Fig. 26, 29a Note 2
E_{OFF}	Turn Off Switching Energy (Body Diode FWD)		1.1				
$t_{d(on)}$	Turn-On Delay Time		68		ns	V_{DD} = 1200 V, V_{GS} = -5/20 V I_D = 50 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	Fig. 27, 29 Note 2
t_r	Rise Time		19				
$t_{d(off)}$	Turn-Off Delay Time		35				
t_f	Fall Time		19				
$R_{G(int)}$	Internal Gate Resistance		1.3		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		43		nC	V_{DS} = 1200 V, V_{GS} = -5/20 V I_D = 50 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		74				
Q_g	Total Gate Charge		200				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 1200V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 1200V

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.8		V	V_{GS} = - 5 V, I_{SD} = 25 A	Fig. 8, 9, 10 Note 1
		3.4		V	V_{GS} = - 5 V, I_{SD} = 25 A, T_J = 150 °C	
I_S	Continuous Diode Forward Current		76	A	V_{GS} = - 5 V, T_C= 25 °C	Note 1
$I_{S,\ pulse}$	Diode pulse Current		160	A	V_{GS} = - 5 V, pulse width t_P limited by T_{jmax}	Note 1
t_{rr}	Reverse Recovery Time	53		ns	V_{GS} = - 5 V, I_{SD} = 50 A , V_R = 1200 V dif/dt = 1000 A/µs, T_J = 150 °C	
Q_{rr}	Reverse Recovery Charge	461		nC		
I_{rrm}	Peak Reverse Recovery Current	14		A		
t_{rr}	Reverse Recovery Time	40		ns	V_{GS} = - 5 V, I_{SD} = 50 A , V_R = 1200 V dif/dt = 3040 A/µs, T_J = 150 °C	
Q_{rr}	Reverse Recovery Charge	481		nC		
I_{rrm}	Peak Reverse Recovery Current	22		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{θJC}$	Thermal Resistance from Junction to Case	0.25	0.37	°C/W		Fig. 21
$R_{θJC}$	Thermal Resistance from Junction to Ambient		40			

Typical Performance

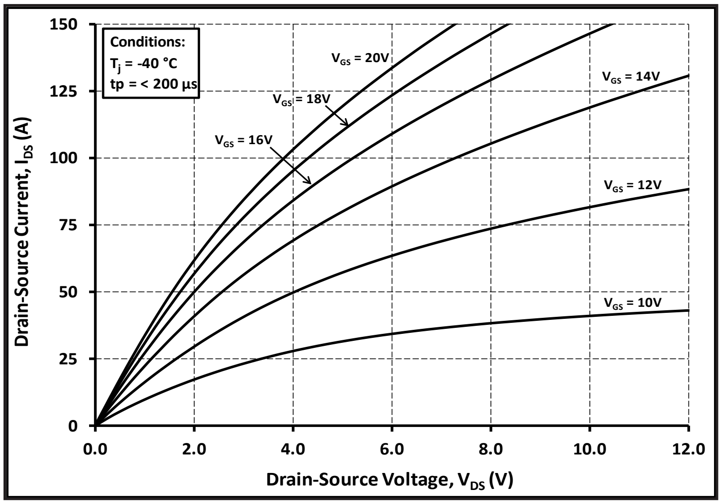


Figure 1. Output Characteristics T_J = -40 °C

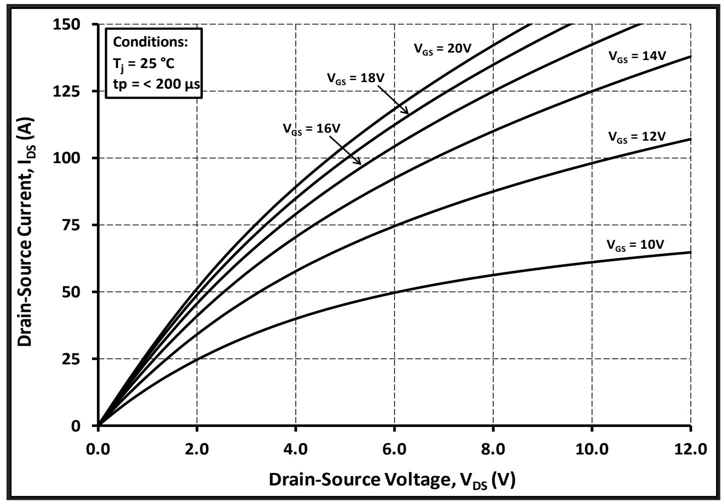


Figure 2. Output Characteristics T_J = 25 °C

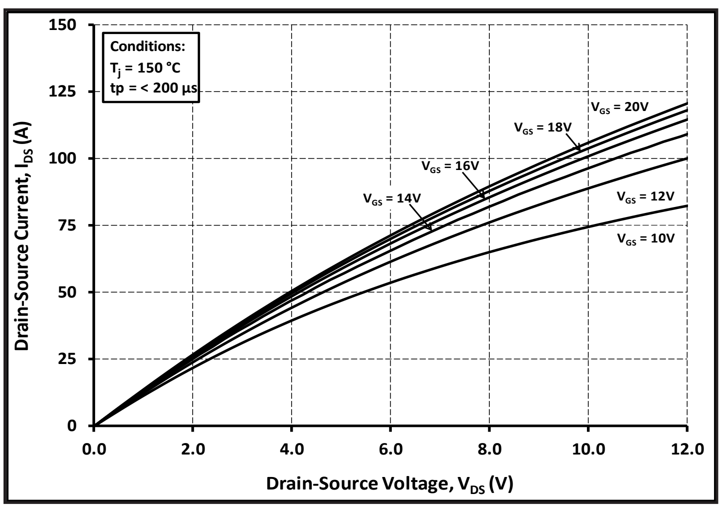


Figure 3. Output Characteristics T_J = 150 °C

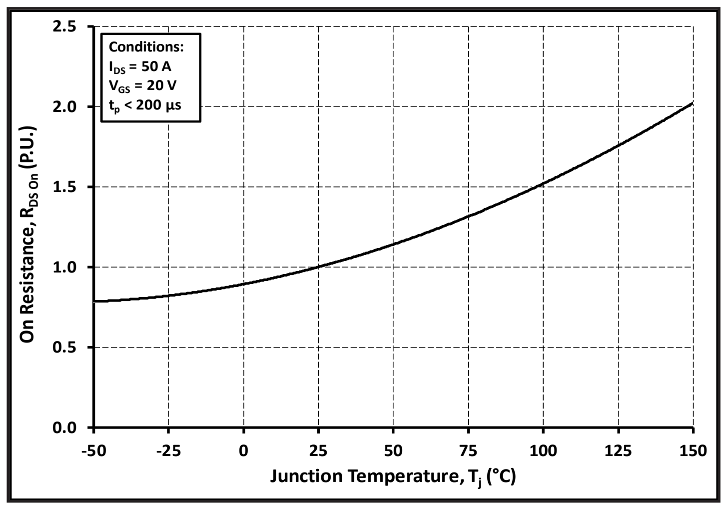


Figure 4. Normalized On-Resistance vs. Temperature

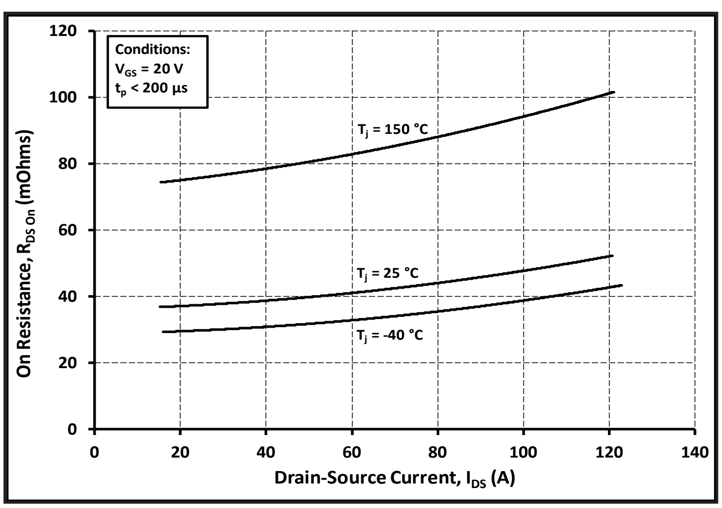


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

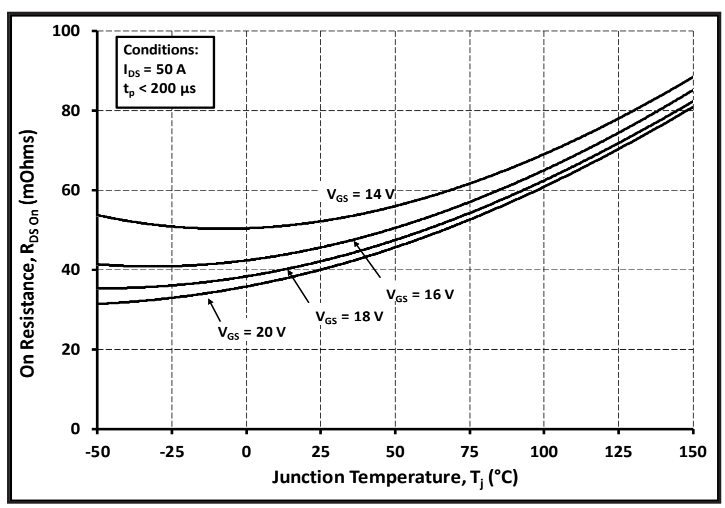


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

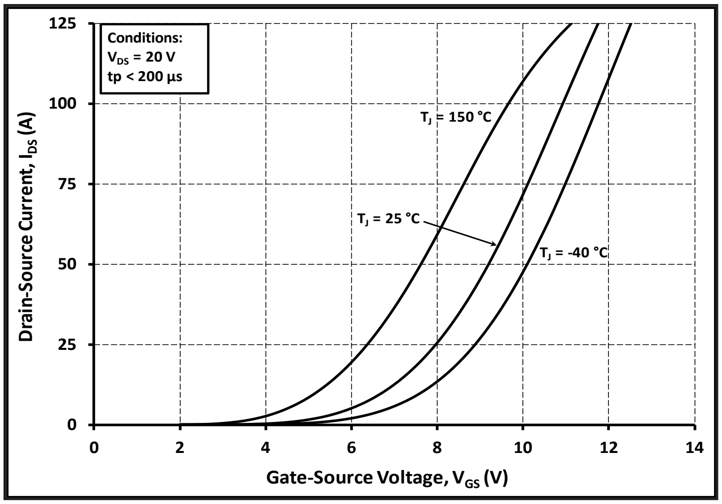


Figure 7. Transfer Characteristic For Various Junction Temperatures

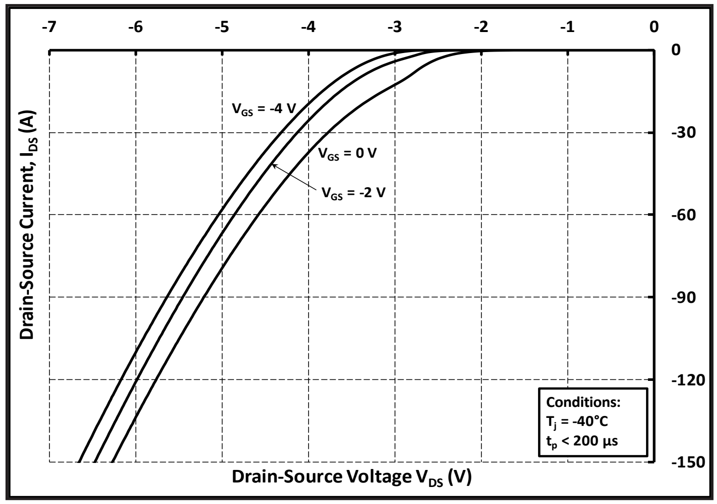


Figure 8. Body Diode Characteristic at -40 °C

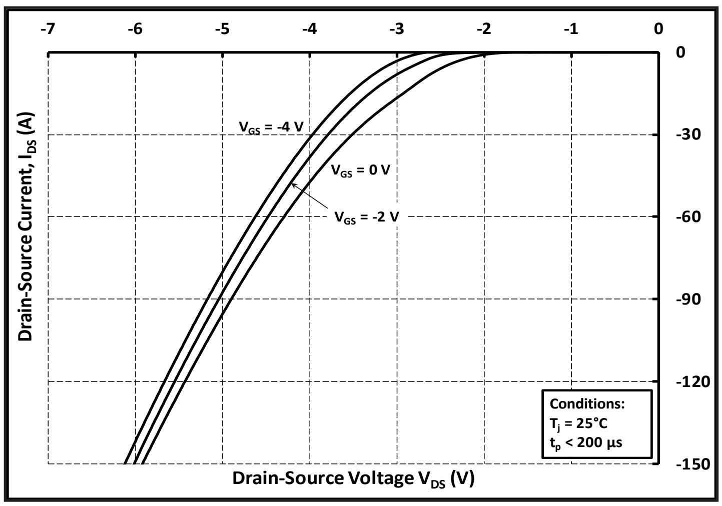


Figure 9. Body Diode Characteristic at 25 °C

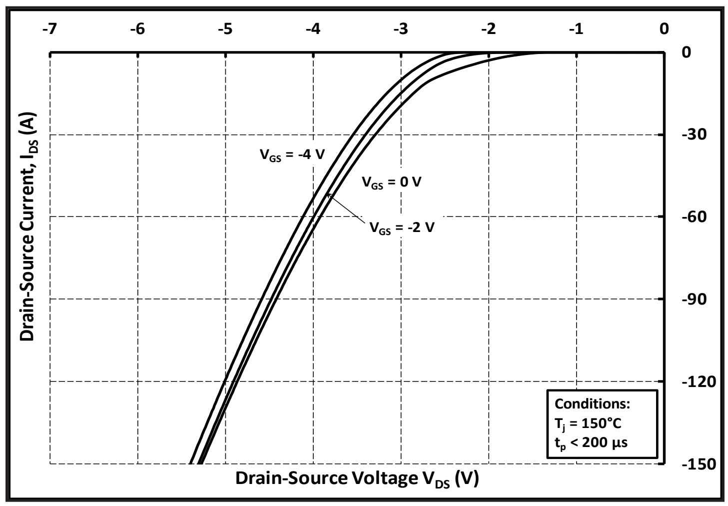


Figure 10. Body Diode Characteristic at 150 °C

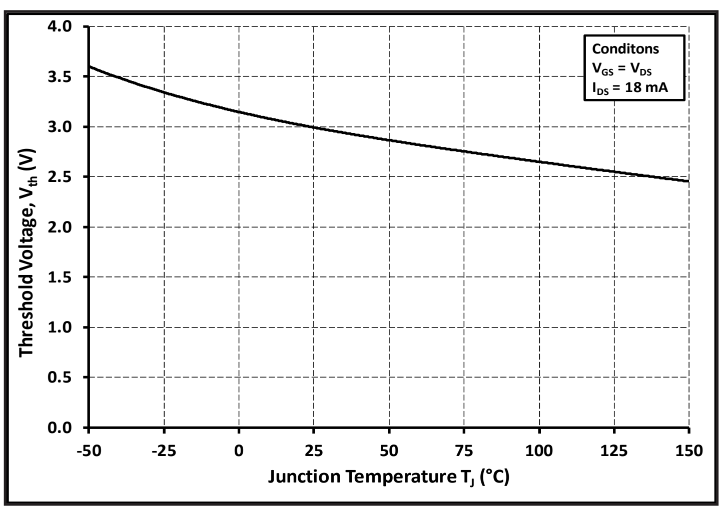


Figure 11. Threshold Voltage vs. Temperature

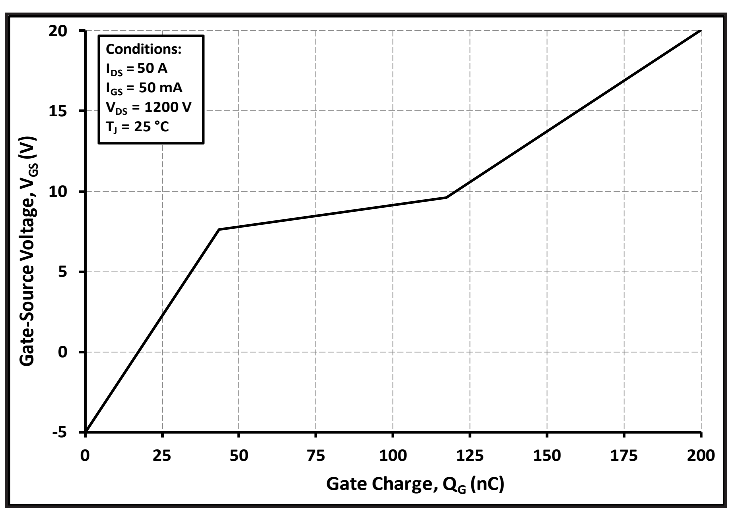


Figure 12. Gate Charge Characteristic

Typical Performance

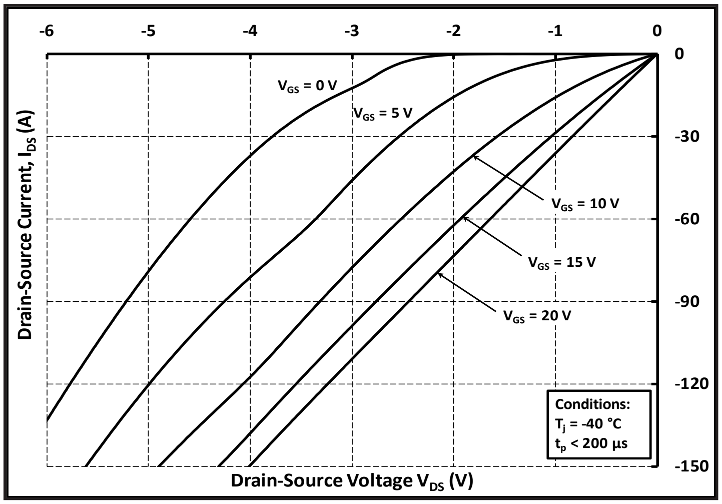


Figure 13. 3rd Quadrant Characteristic at -40 °C

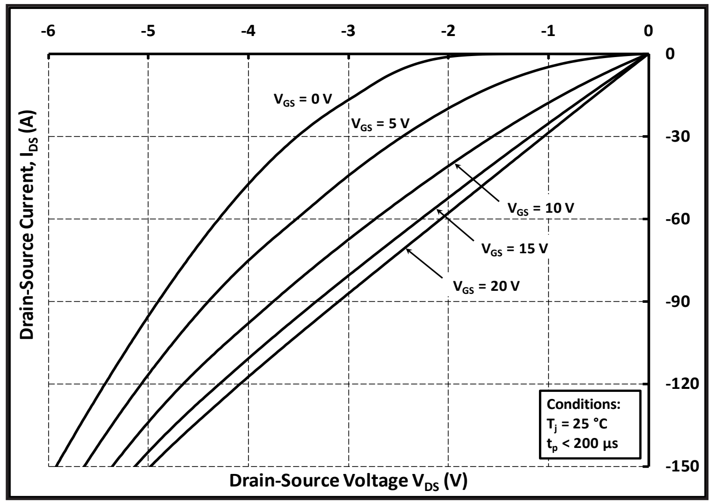


Figure 14. 3rd Quadrant Characteristic at 25 °C

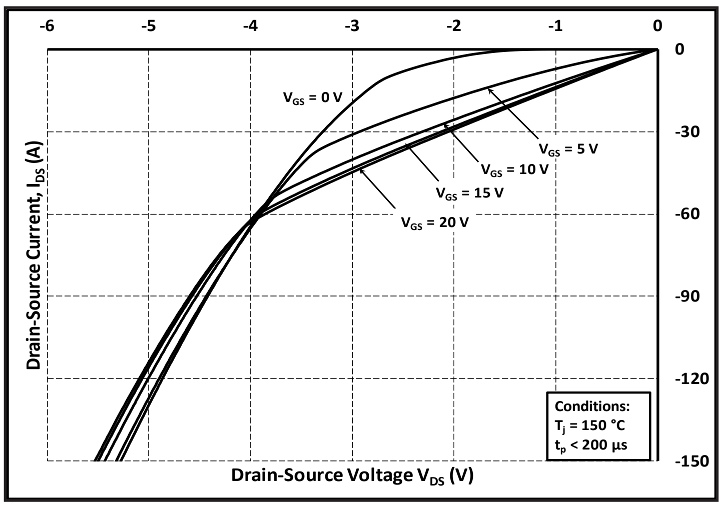


Figure 15. 3rd Quadrant Characteristic at 150 °C

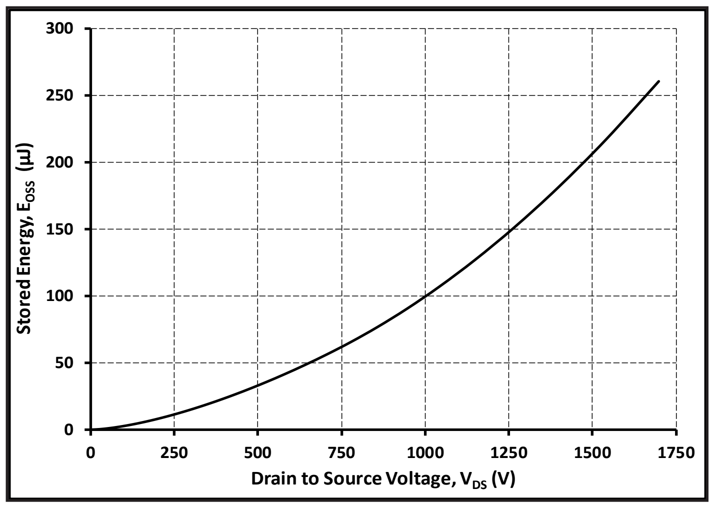


Figure 16. Output Capacitor Stored Energy

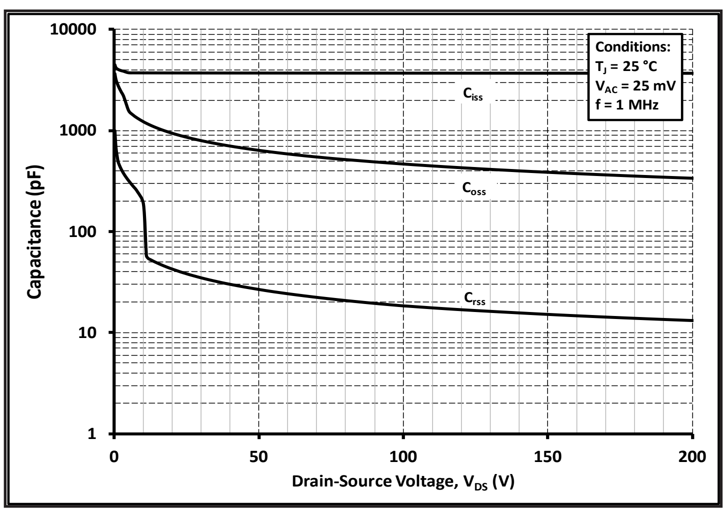


Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

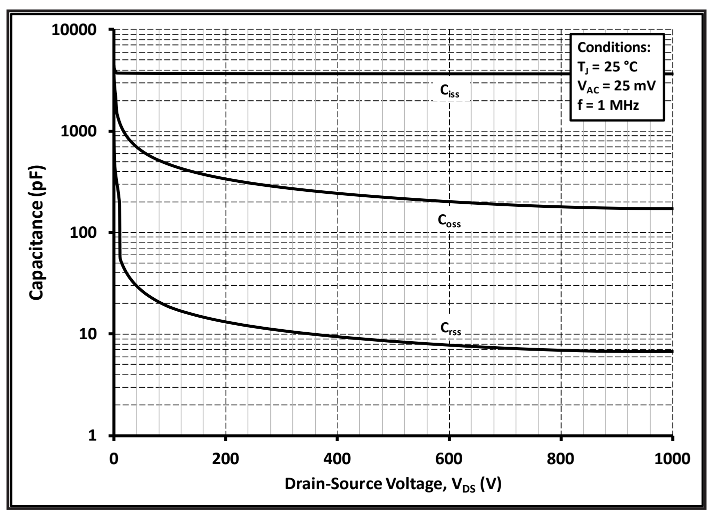


Figure 18. Capacitances vs. Drain-Source Voltage (0-1000 V)

Typical Performance

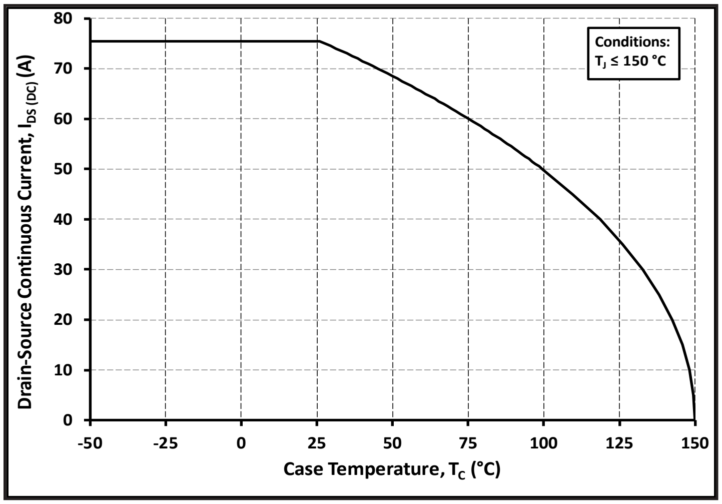


Figure 19. Continuous Drain Current Derating vs. Case Temperature

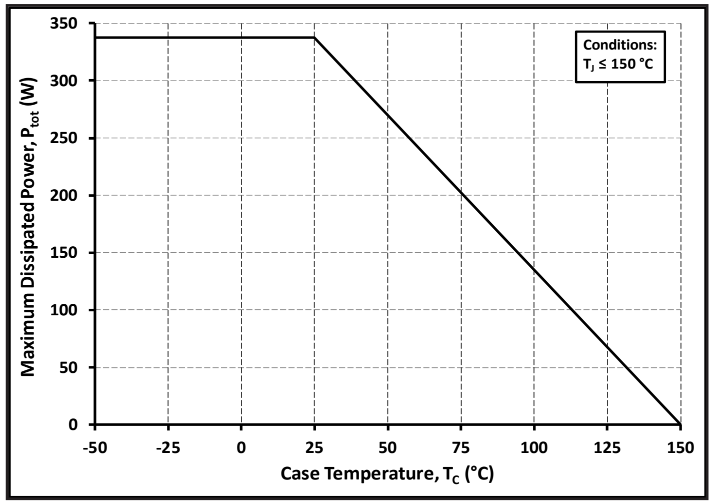


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

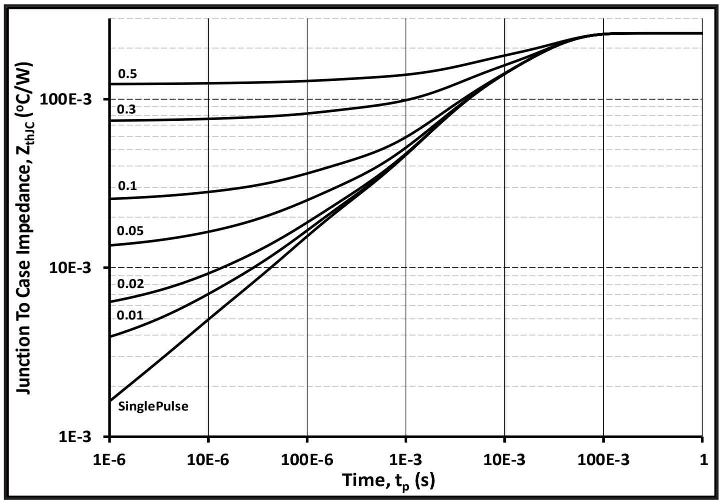


Figure 21. Transient Thermal Impedance (Junction - Case)

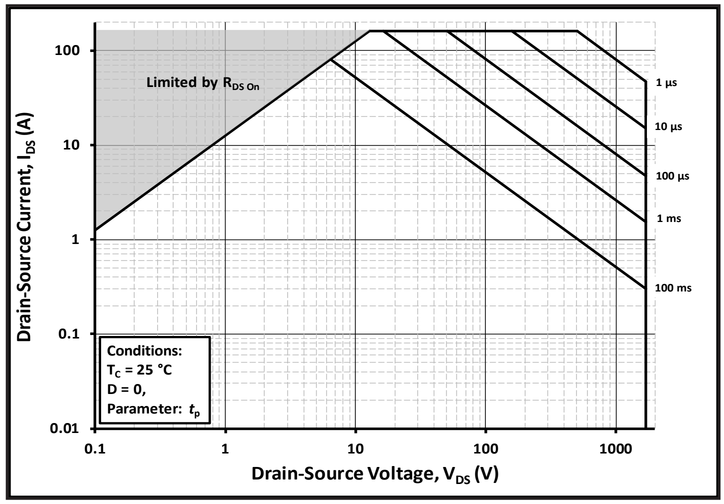


Figure 22. Safe Operating Area

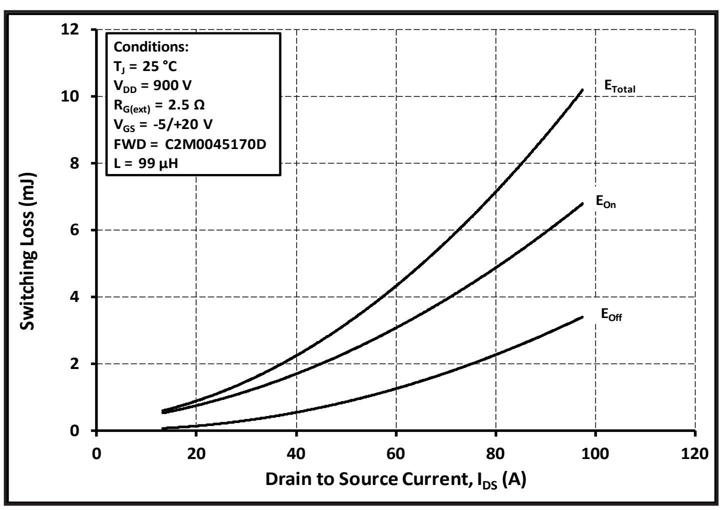


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 900V)

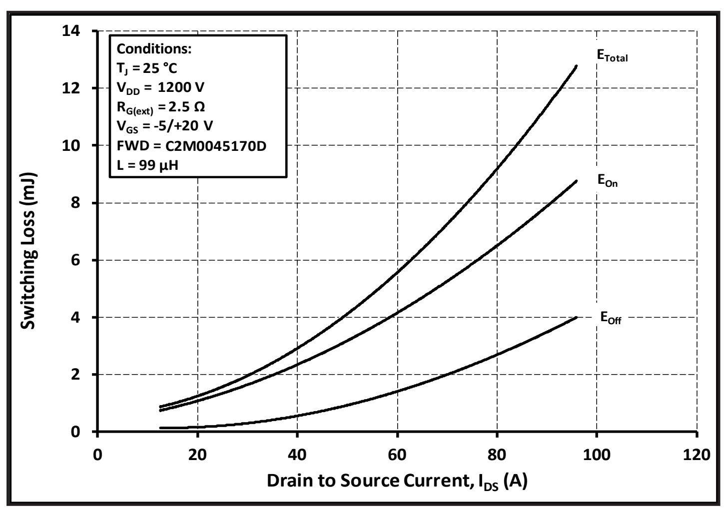


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 1200V)

Typical Performance

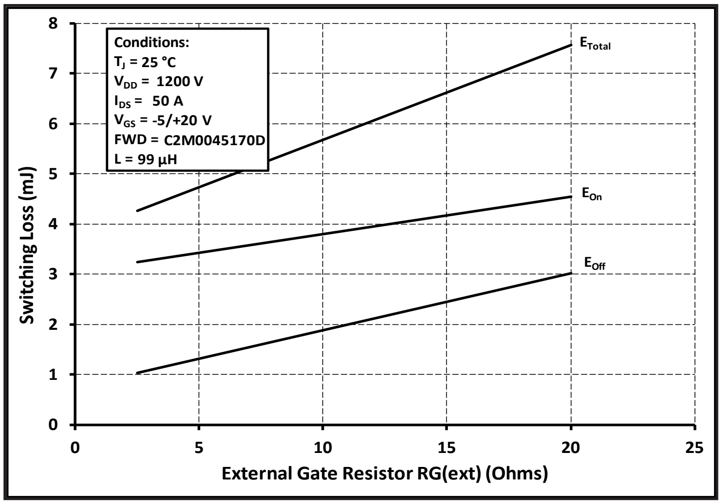


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

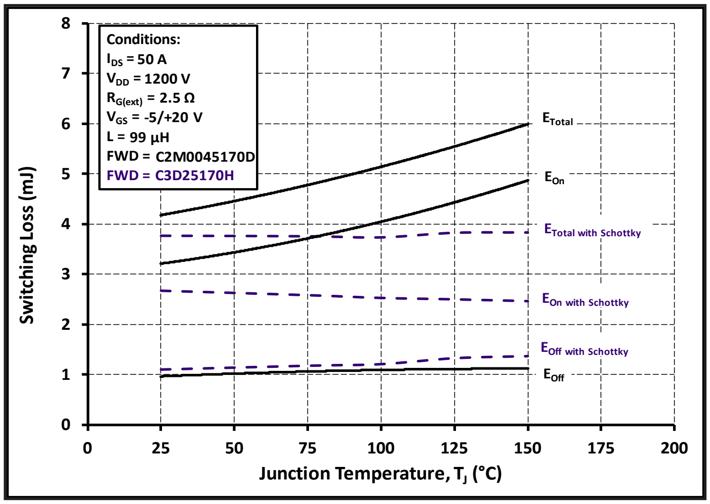


Figure 26. Clamped Inductive Switching Energy vs. Temperature

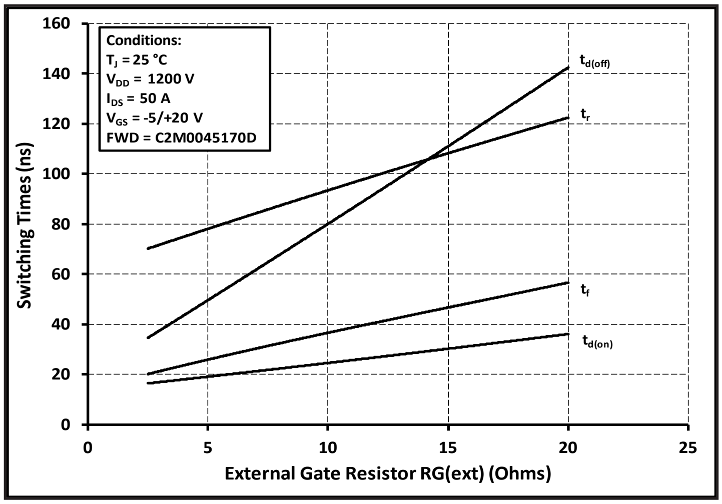


Figure 27. Switching Times vs. $R_{G(ext)}$

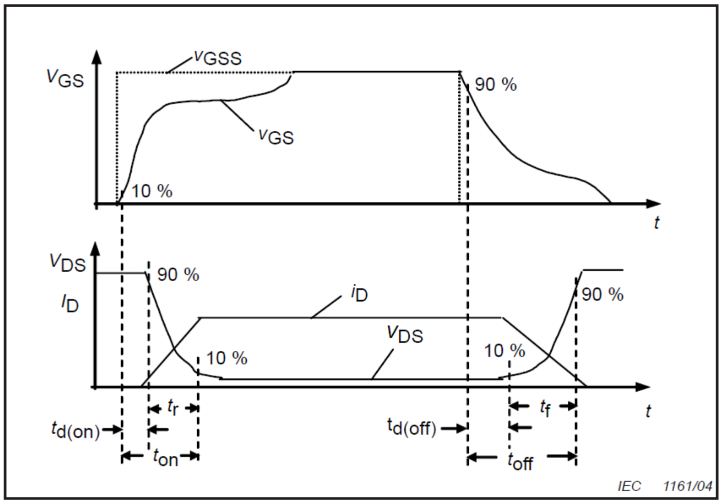


Figure 28. Switching Times Definition

Test Circuit Schematic

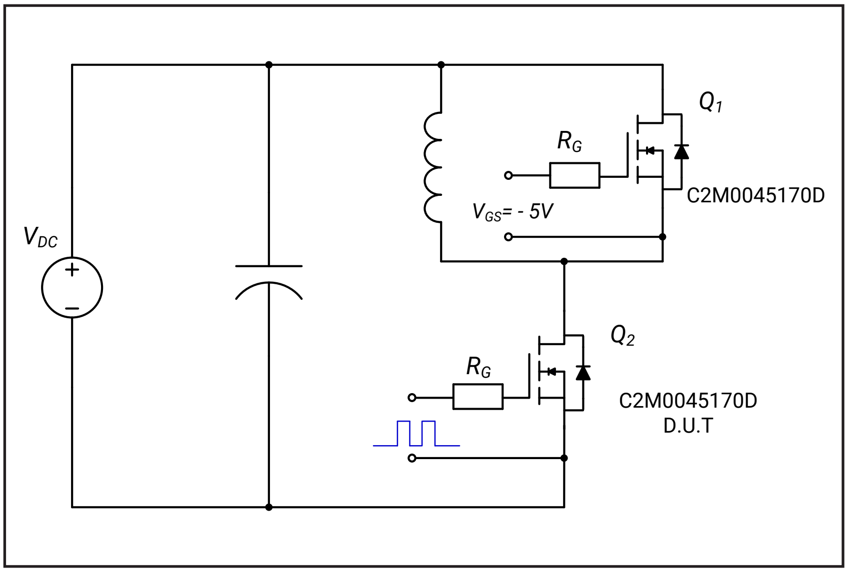


Figure 29a. Clamped Inductive Switching Test Circuit using
MOSFET intristic body diode

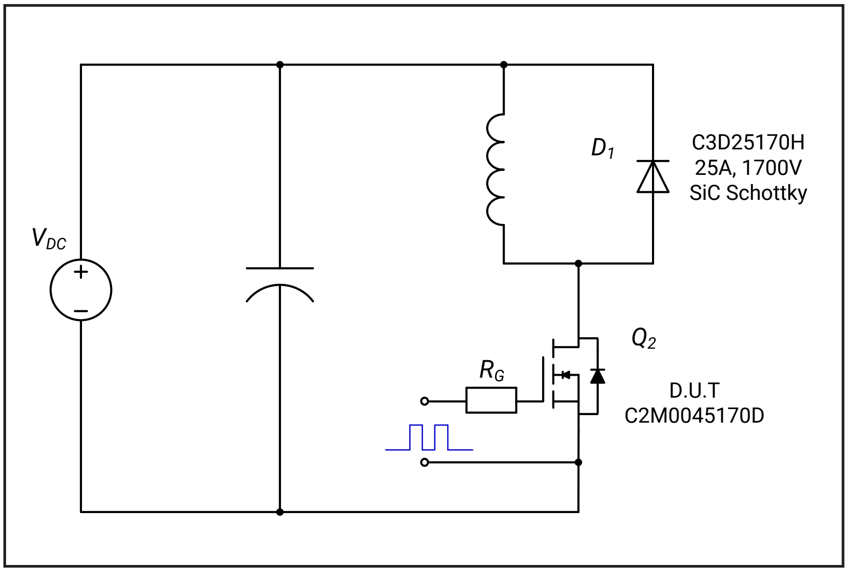
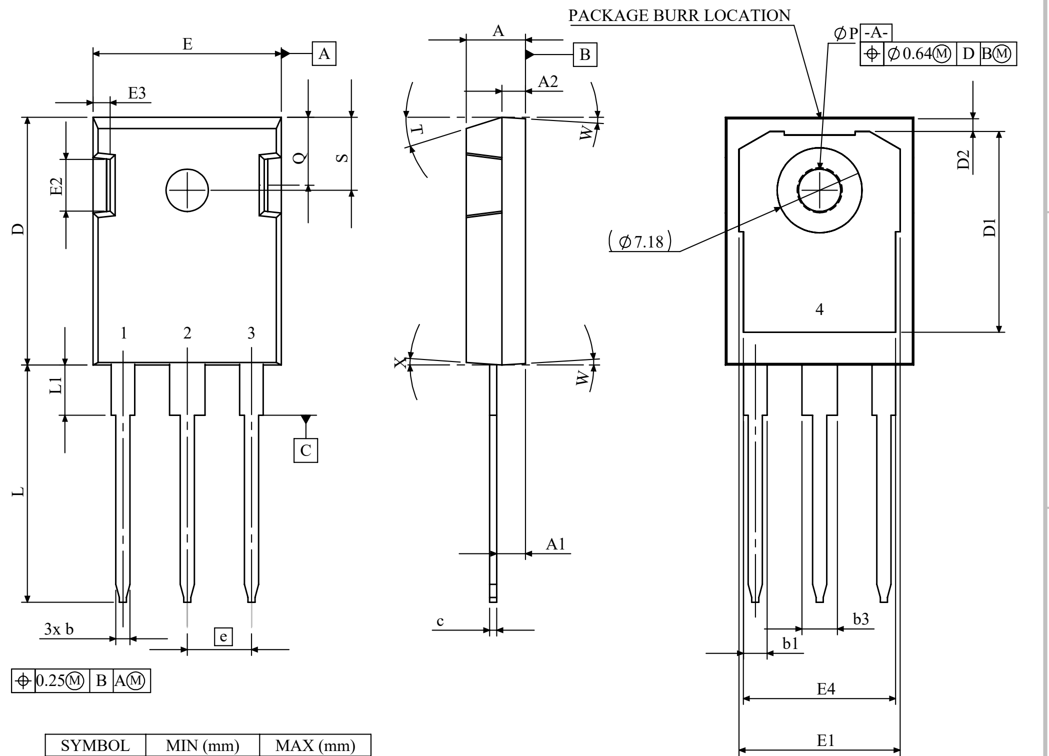


Figure 29b. Clamped Inductive Switching Test Circuit using
SiC Schottky diode

Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b	1.07	1.33
b1	1.91	2.41
b3	2.87	3.38
c	0.55	0.68
D	20.8	21.1
D1	16.25	17.65
D2	0.95	1.25
E	15.75	16.13
E1	13.1	14.15
E2	3.68	5.1
E3	1	1.9
E4	12.38	13.43
e	5.44 BSC	
L	19.81	20.32
L1	4.1	4.4
ØP	3.51	3.65
Q	5.49	6
S	6.04	6.3
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	GATE
2	DRAIN
3	SOURCE
4	DRAIN

NOTES:
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

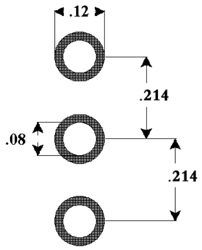
TITLE: PACKAGE OUTLINE DRAWING: TO-247-3L(MOSFET)

Date: 04/13/22

REVISION NO. 01 A4

SCALE:1:1 SHEET 1 OF 1

Recommended Solder Pad Layout



TO-247-3

Revision history

Document Version	Date of release	Descriptiion of changes
Rev -	June - 2016	Initial datasheet
Rev 1	May - 2022	Added effective output capacitance, Typical values updated to support PCN-1278.

Note:

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